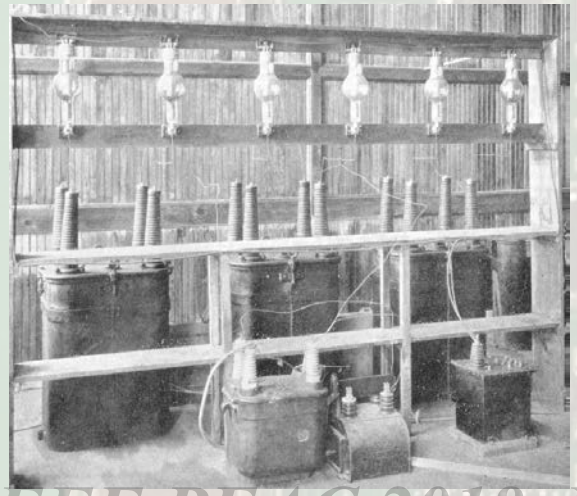
Architectures and Topologies for High-Frequency, High-Density Power Conversion

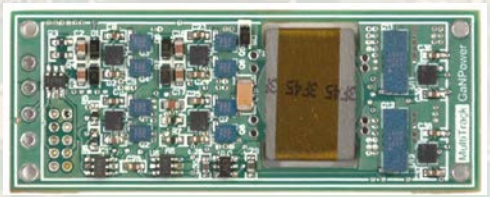
Power Electronics and Applications Conference

Shenzhen, China – November 2018

David Perreault



20 kW Kenotron Rectifier, Circa 1926
(From Principles of Rectifier Circuits, Prince and Vogdes, McGraw Hill 1927)



Isolated Power Supply, Circa 2016
(Minjie Chen, MIT)

??

Circa 2026

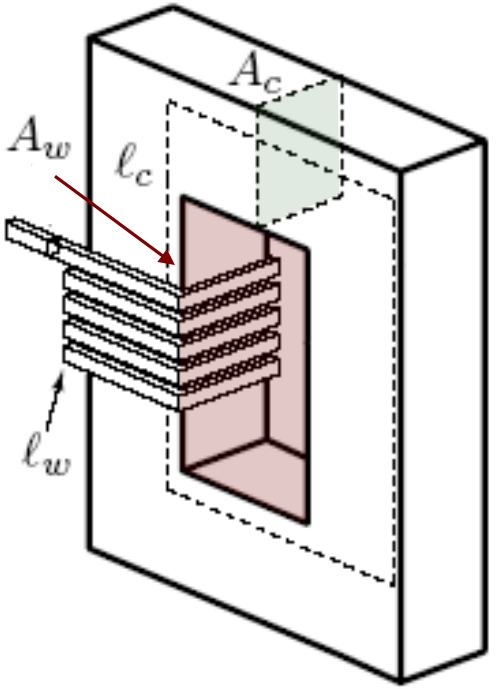
Passive Components Dominate

- **Power electronics systems are dominated by *passives* (especially magnetics*)***
- **Demonstration design by EPC from ECCE 2015**
  - **300 kHz Telecom converter design based on EPC eGaN FETs**
  - **Magnetics ~48% of loss, 45% of Area**

- **Commercial LED Driver (cooper)**
  - **~ 100 kHz , 4.8 W/in^3**
  - **>90% passives by volume**

Miniaturizing Magnetics is Difficult

- **Scaling laws work *against* miniaturization of power magnetics**
  - **Simplified case: power handling (VA) of a fixed-frequency inductor**
    - **Flux density B_0 limited by core loss**
    - **Current density J_0 limited by winding loss**
- **If we scale dimensions by factor ε**
  - **Areas scale as ε^2**
  - **Volumes scale as ε^3**
  - **Power handling as ε^4, *faster* than volume**
- **Power *density* scales as ε**
  - **Gets worse at smaller size!**



$$VA = V \cdot I \propto (N f B_0 A_C) \cdot \left(\frac{J_0 A_W}{N}\right) = f \cdot B_0 \cdot J_0 \cdot (A_C A_W)$$

Sullivan, et. al., "On Size and Magnetics: Why Small Efficient Power Inductors are Rare," *International Symposium on 3D Power Electronics Integration and Manufacturing*, June 2016

Opportunities for Advances

- **Improvements in semiconductor devices, integrated circuits / controls, magnetic materials and packaging open the door to better power electronics**

- **More *sophisticated* converter designs now possible**
  - **Better leverage the way we use passives to greatly improve size, efficiency and performance**

- **Much *higher-frequency* converters now possible**
  - **(10-100x higher than conventional approaches)**
  - **Substantial reductions in energy storage / passives**

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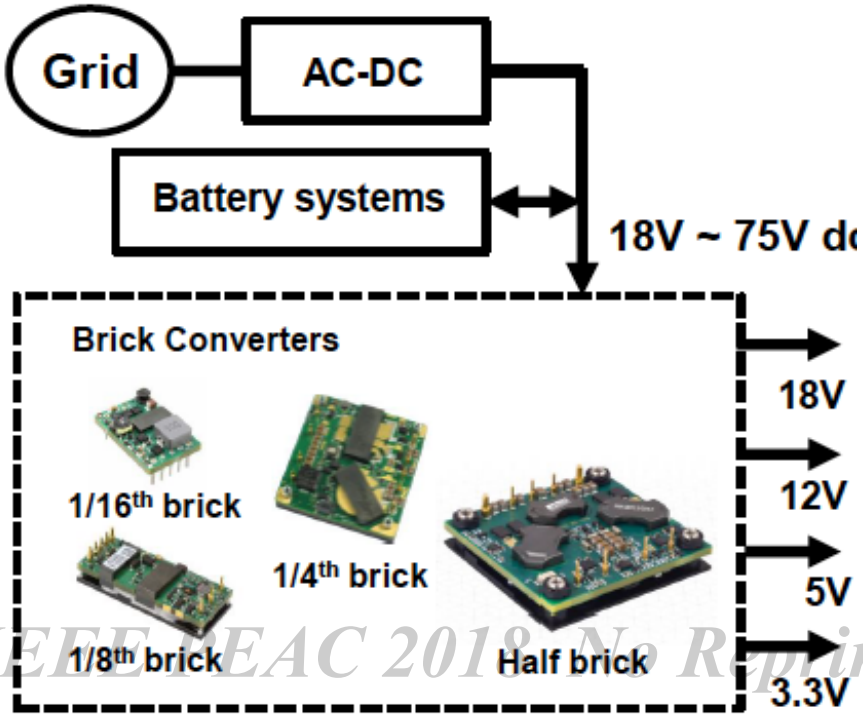
New System Architectures and Topologies

- **Power electronics design has historically been driven by a desire (and need) for simplicity**
- **Advances in semiconductor devices, integrated circuits, controls and passive integration techniques favor adoption of more sophisticated power conversion approaches**
- **We should *judiciously* utilize higher complexity to leverage technology advances**
  - **Smaller, more efficient and higher-performance solutions**

- **We can accomplish this by leveraging:**
  - **Designs that reduce magnetic energy storage requirements**
  - **Controls enabling very wide operating ranges at low device and component stress (e.g., via mode changes)**

Example #1: Telecom Converter

- **All kinds of electronic equipment require isolated dc-dc power converters operating from wide range inputs to low-voltage outputs**
  - **Servers in data centers**
  - **Telecommunications**

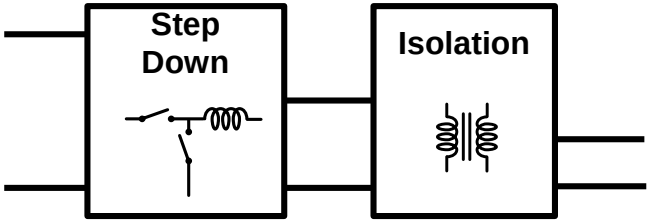


Requirements

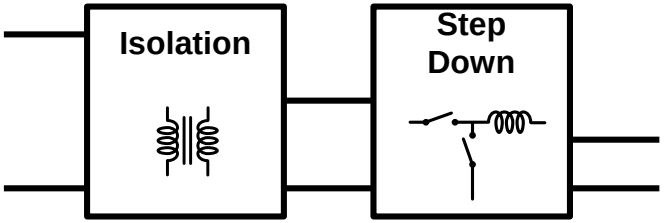
- Wide Input Voltage Range
- High Voltage Conversion Ratio
- High Power Density
- Galvanic Isolation
- High Efficiency
- Low Cooling Requirement

Typical Solutions

Buck + Isolation



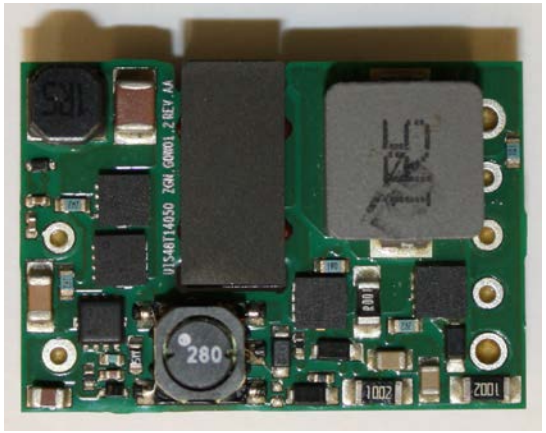
Forward Converter

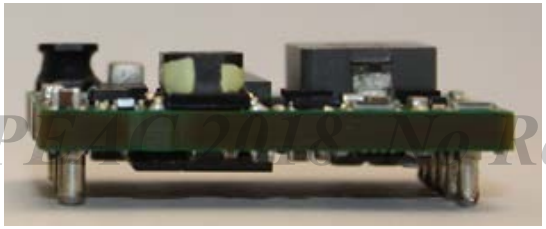


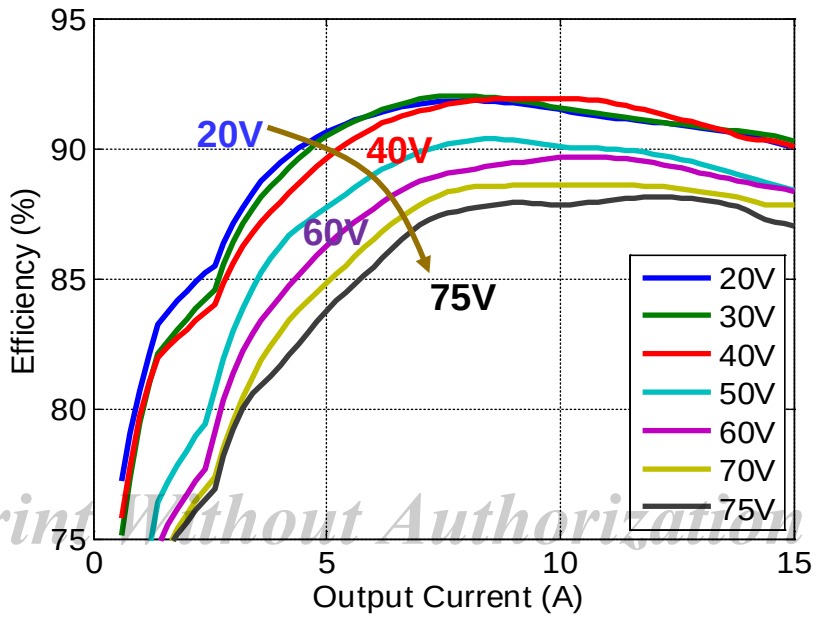
Best commercial 1/16th brick wide-input dc-dc converter

Simple structure but has multiple large magnetic components

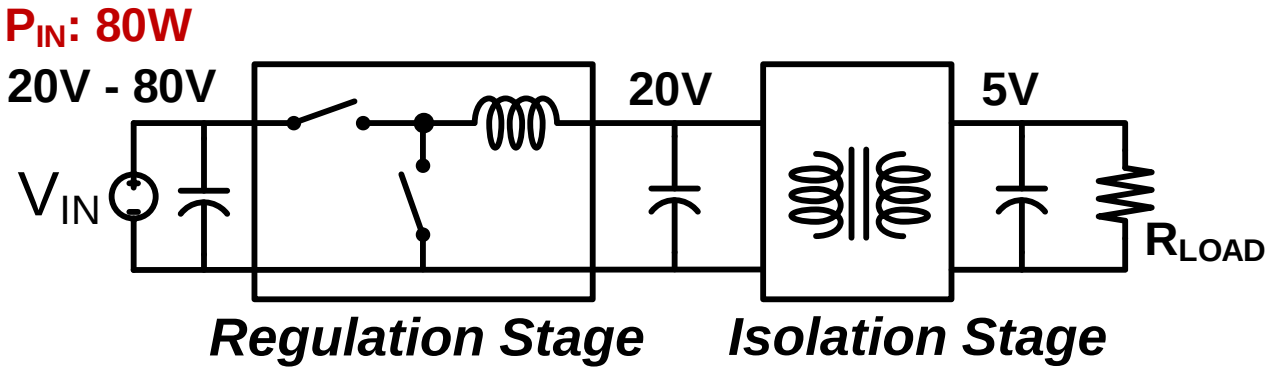
18 V - 75 V_{in}
5 V_{out}
75 W
1/16 brick
isolated







Conventional Two-Stage Dc-Dc Architecture

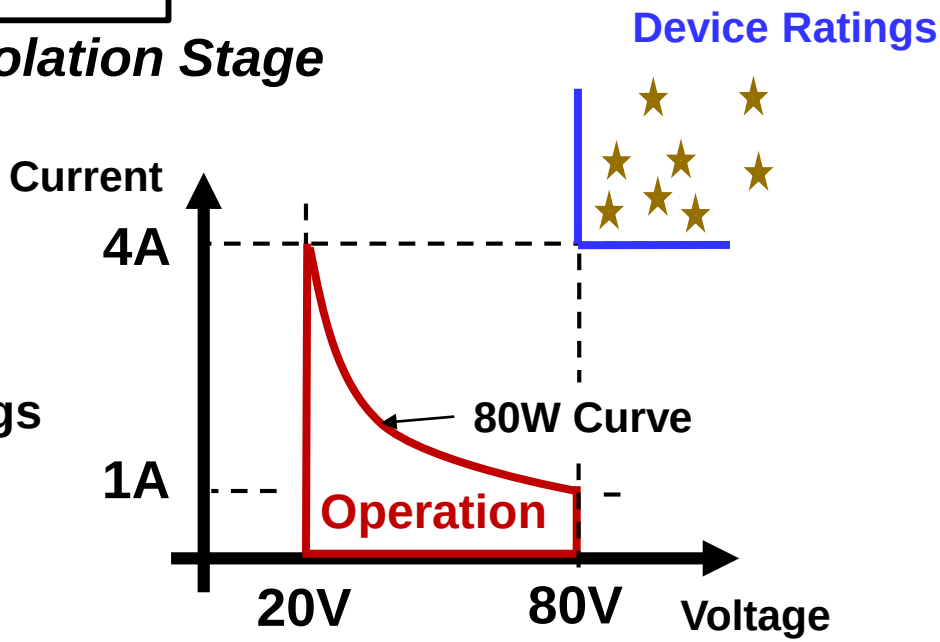


Cost of Switch Ratings

1. High voltage rating → resistance
2. High current rating → die area

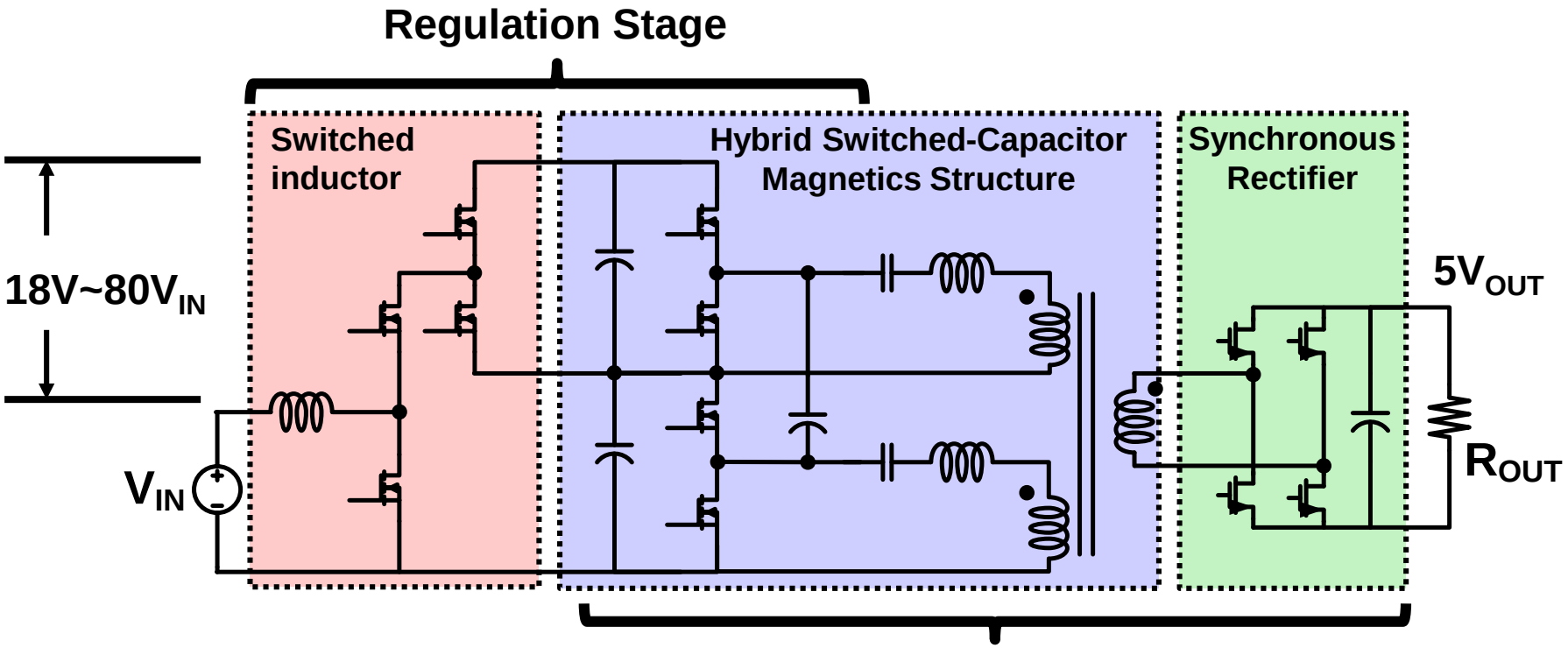
Cost of Passive Component Ratings

1. High capacitance → volume
2. High inductance → volume

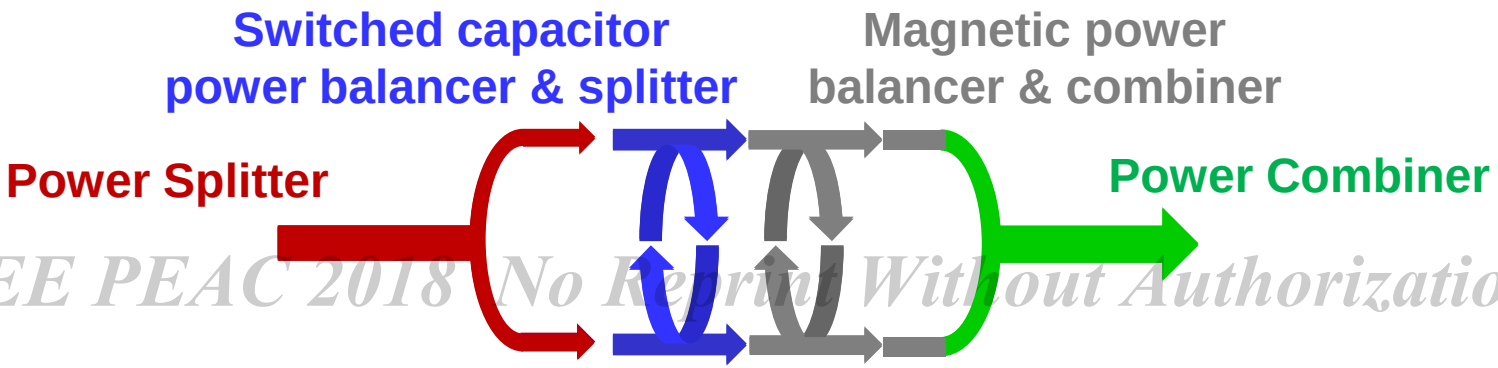


Need to better balance the device rating and the device operational range

MultiTrack Power Conversion Architecture

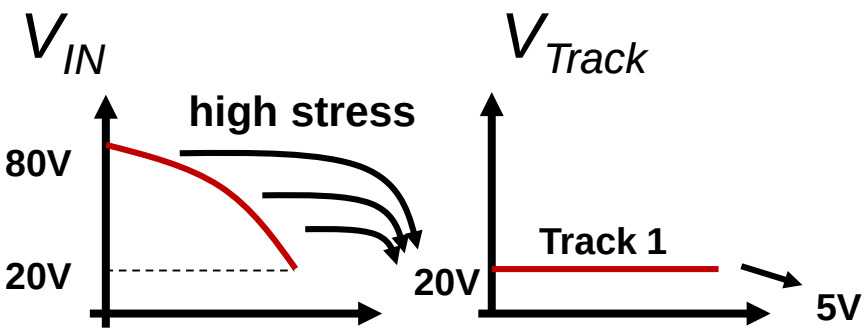


Deliver power in multiple TRACKs

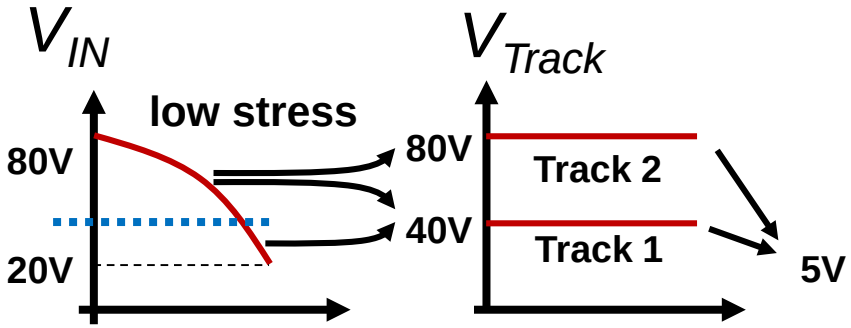


Internal Voltage-Conversion Stress

Single-Track Power Flow



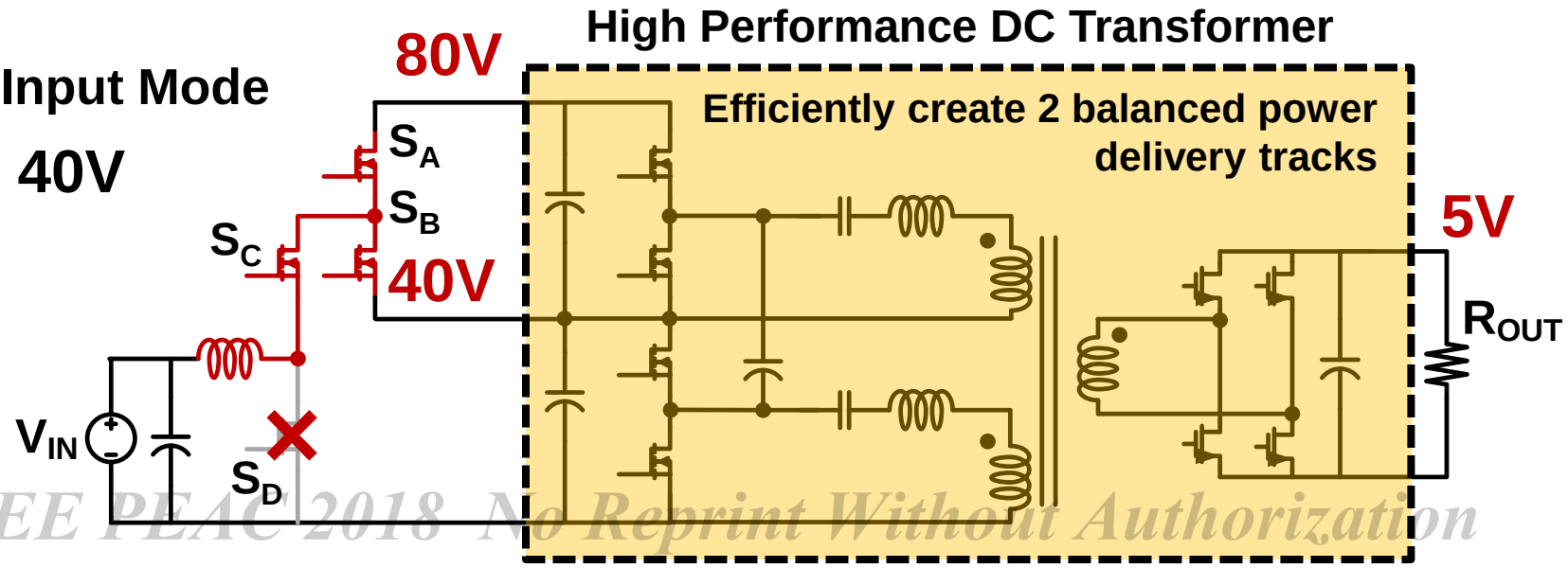
MultiTrack Power Flow



Always deliver power to the closest track

High Input Mode

$V_{IN} > 40V$



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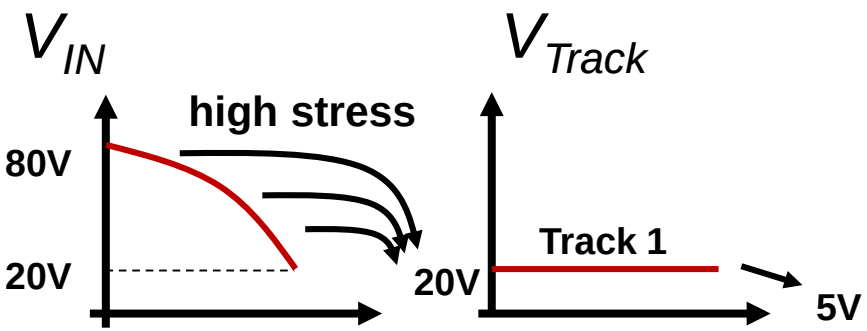
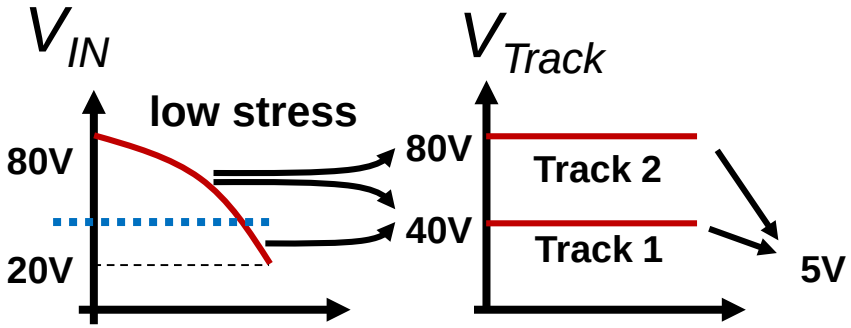


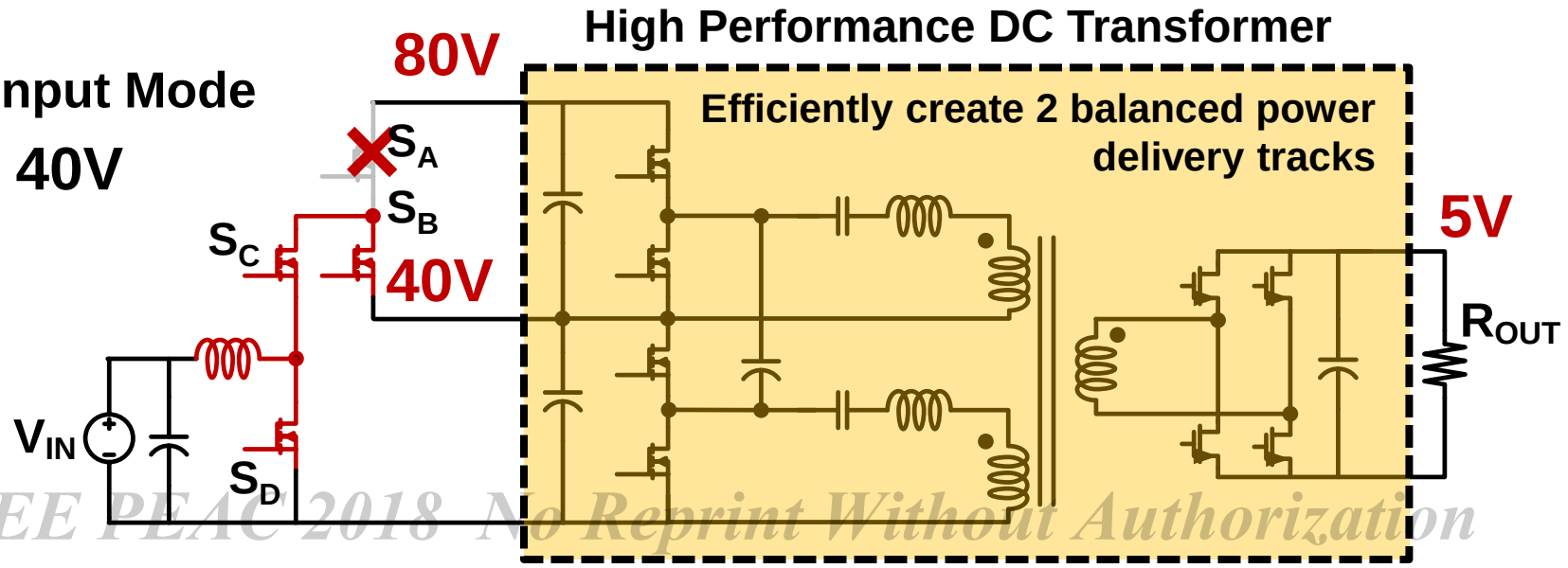
MultiTrack Power Flow



Always deliver power to the closest track

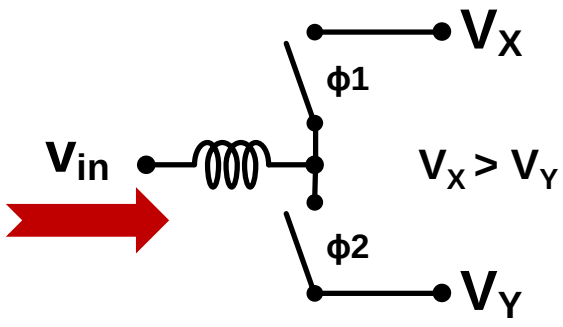
Low Input Mode

$V_{IN} < 40V$



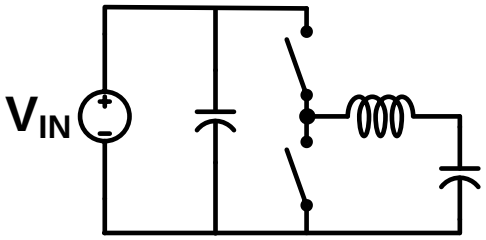
Reduced Inductor Size

Switched-Inductor Unit Cell

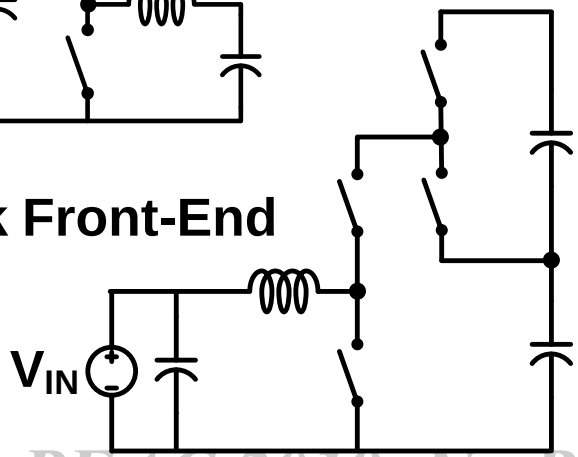


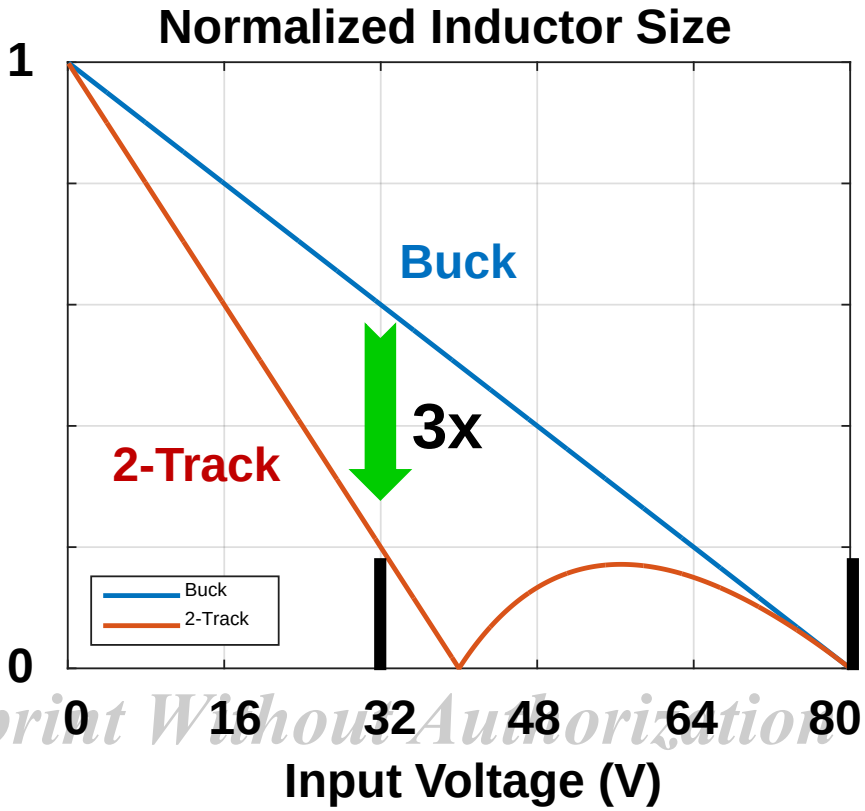
Percentage of energy buffered greatly by the inductor reduced through use of multiple conversion "tracks"

Buck Front-End



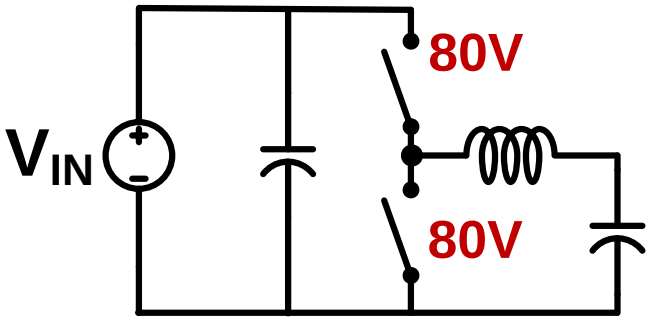
2-Track Front-End





Device Ratings and Conduction Loss

Buck Front-End



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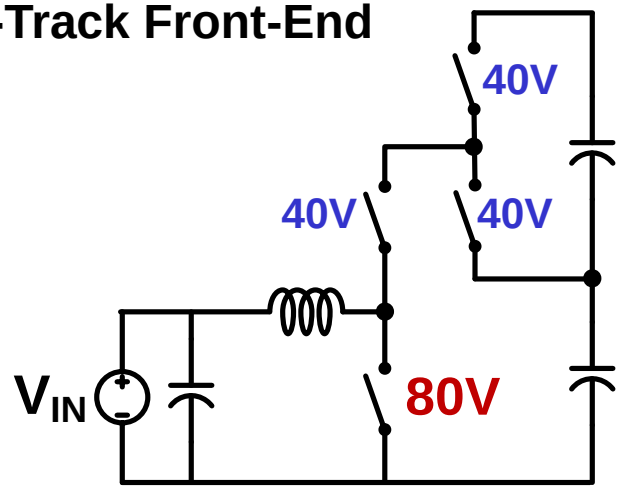
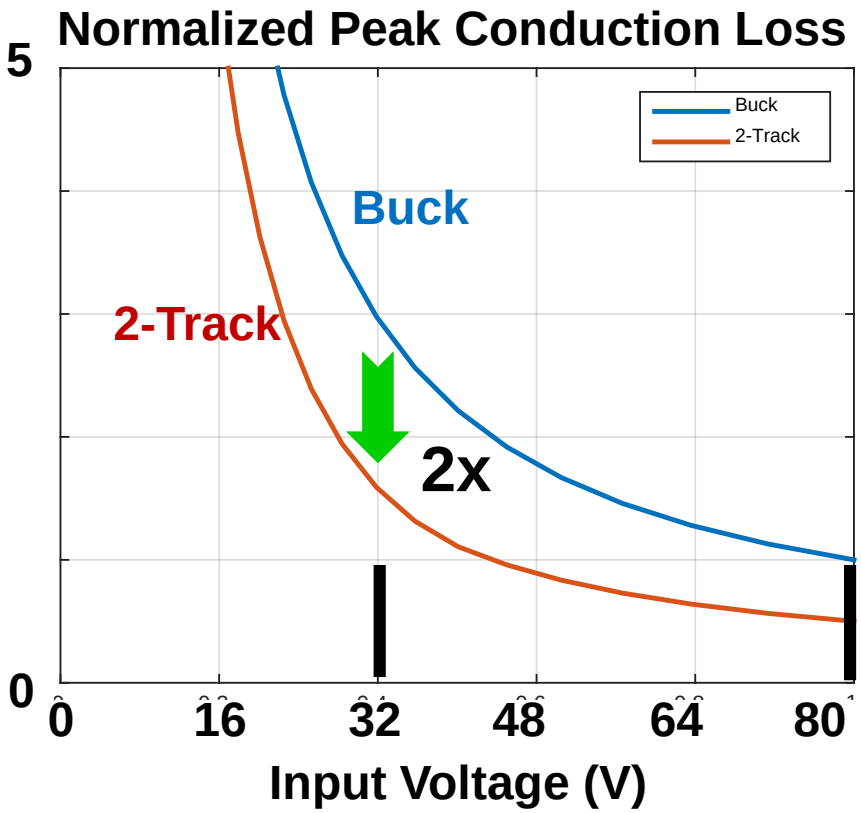


Reduced device voltage rating



- **Favors High Voltage and Potential IC Implementations**
- **Processes power using low voltage rating devices**

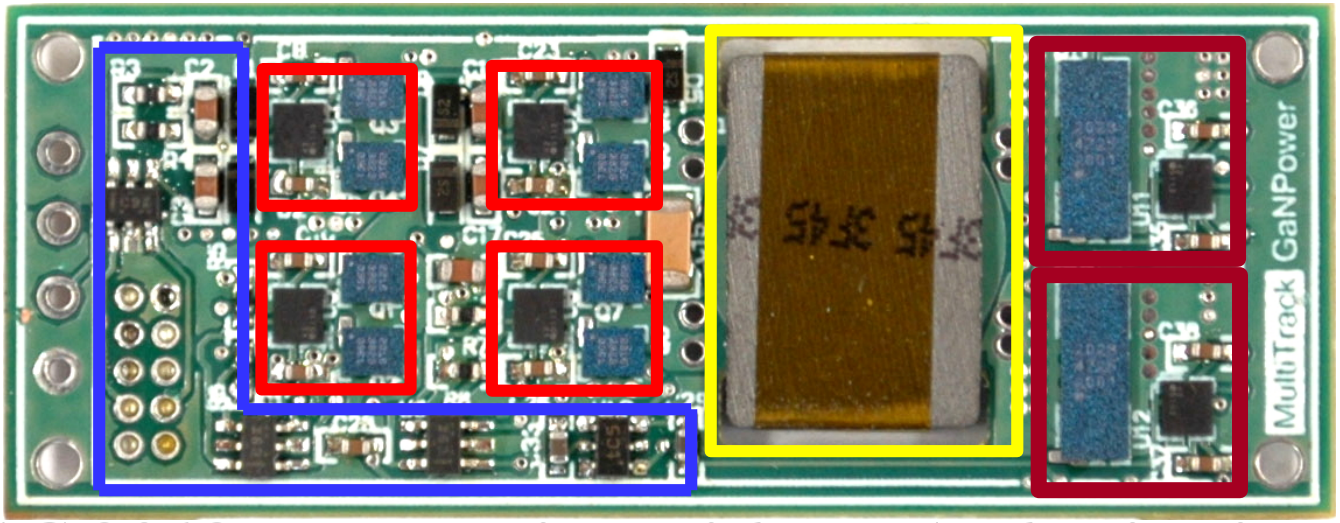
18V-80V, 75W Miniaturized Telecom Converter

- **Resulting design has larger *numbers* of components (switches, drivers, controls) than conventional approaches, but *much lower active and passive component stresses***
- **The converter *structure* is highly modular and manufacturable, and benefits heat transfer**

Modular Input Cells **PCB Integrated Transformer** **Modular Output Cells**

8 Layer PCB with precisely controlled parasitics

Discrete Logic, LDOs, Controls, Signal Buffers, …



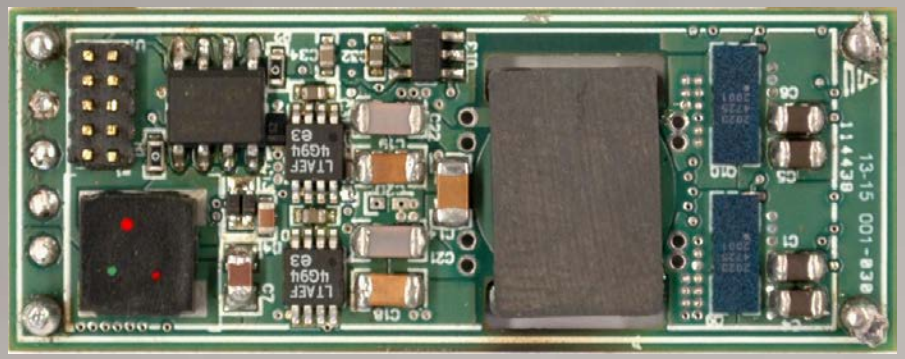
M. Chen, et al "MultiTrack Power Conversion Architecture," *IEEE Transactions on Power Electronics*, Vol. 32, No. 1, pp. 325-340, January 2017.

18V-80V, 75W Miniaturized Telecom Converter

Approach yields better volume, weight and temperature rise

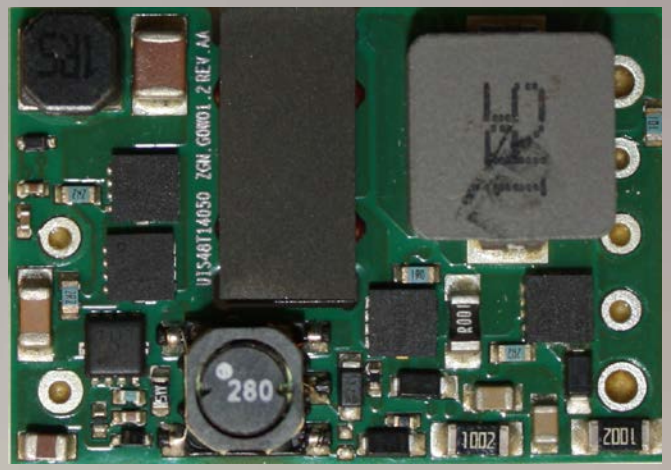
MultiTrack

457.3 W/in^3, 91% **0.93 inch^2**



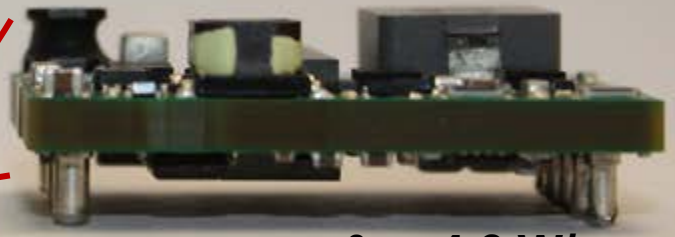
Best commercial product (Forward)

142.5 W/in^3, 91% **1 inch^2**



Overall < 1/3 size, 1/2 weight

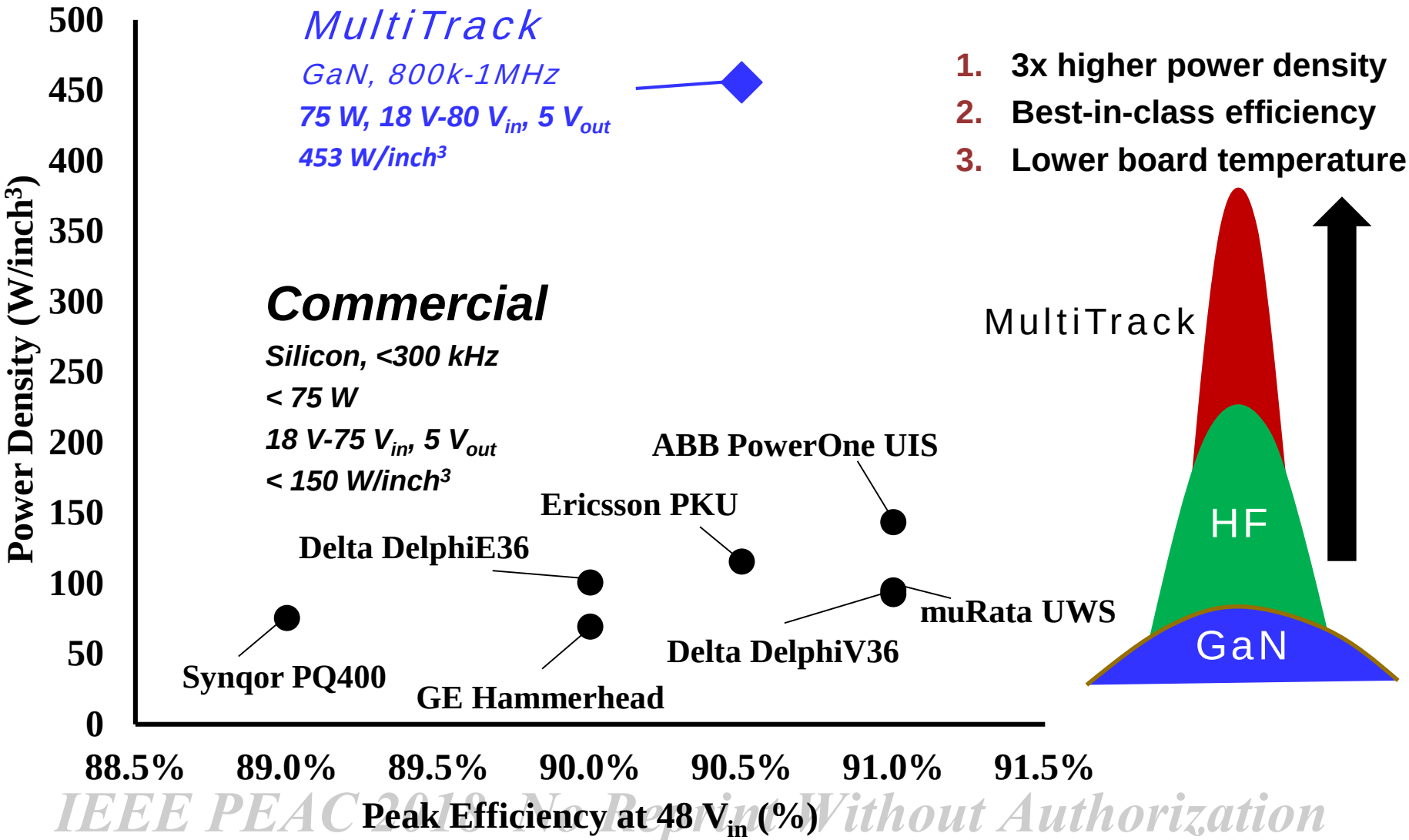
457.3 W/inch^3 **11.5 W/g**



142.5 W/inch^3 **4.6 W/g**

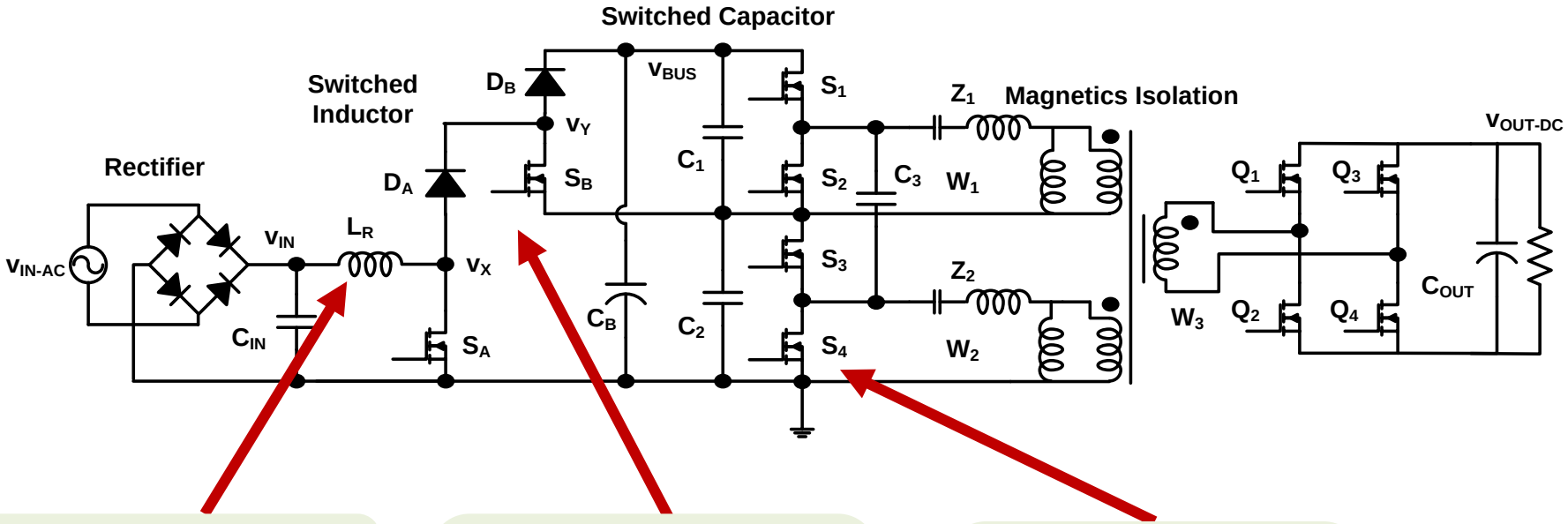
M. Chen, et al "MultiTrack Power Conversion Architecture," *IEEE Transactions on Power Electronics*, Vol. 32, No. 1, pp. 325-340, January 2017.

Benchmark Results



Multitrack PFC

- **The multitrack approach can also be applied to advance performance in other wide-operating-range conversion applications**
  - **E.g., multi-track PFC conversion over universal input**
  - **Similar benefits to components, operating range, construction**



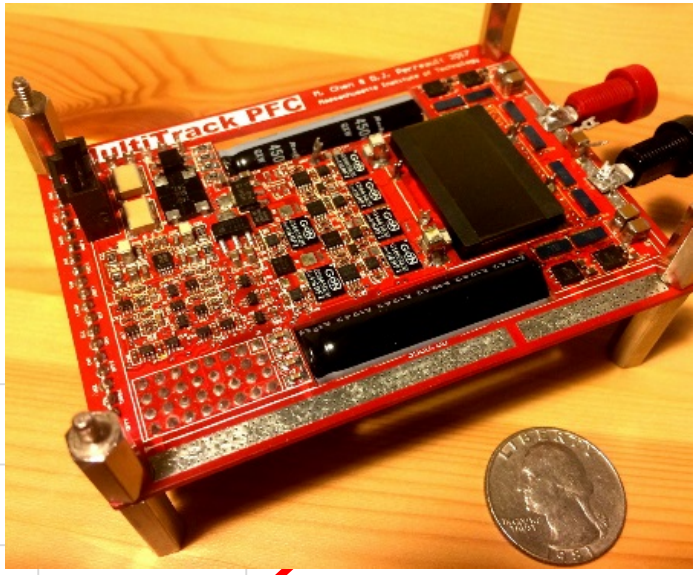
Reduced inductor stress / size

Multiple modes, wide-range ZVS give high efficiency over universal input

Reduced device voltages and transformer ratio

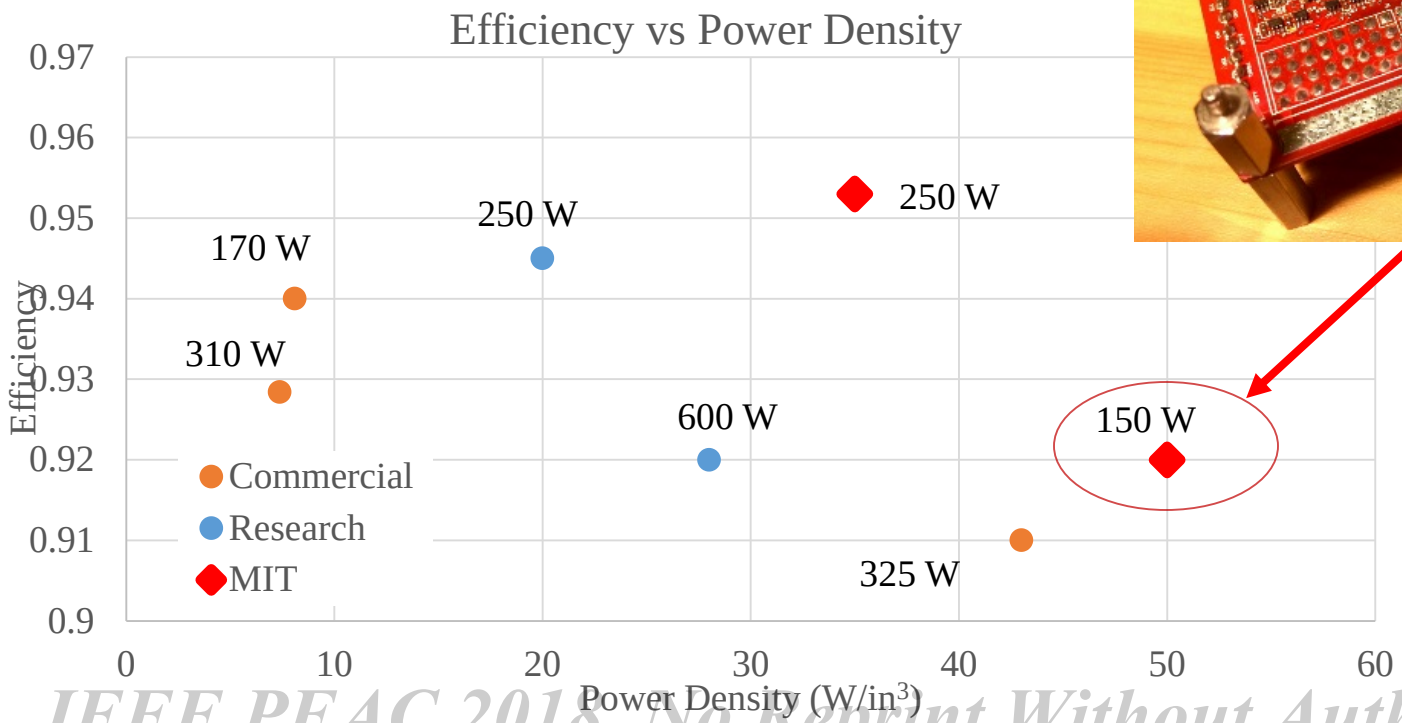
Multitrack PFC

- **First-generation prototype demonstrates the promise of this approach**
  - **150 W, Universal Input, 12 V output**
  - **1-4 MHz switching frequency**
  - **50 W / in^3, 92% efficiency**
  - **MUCH higher performance possible**



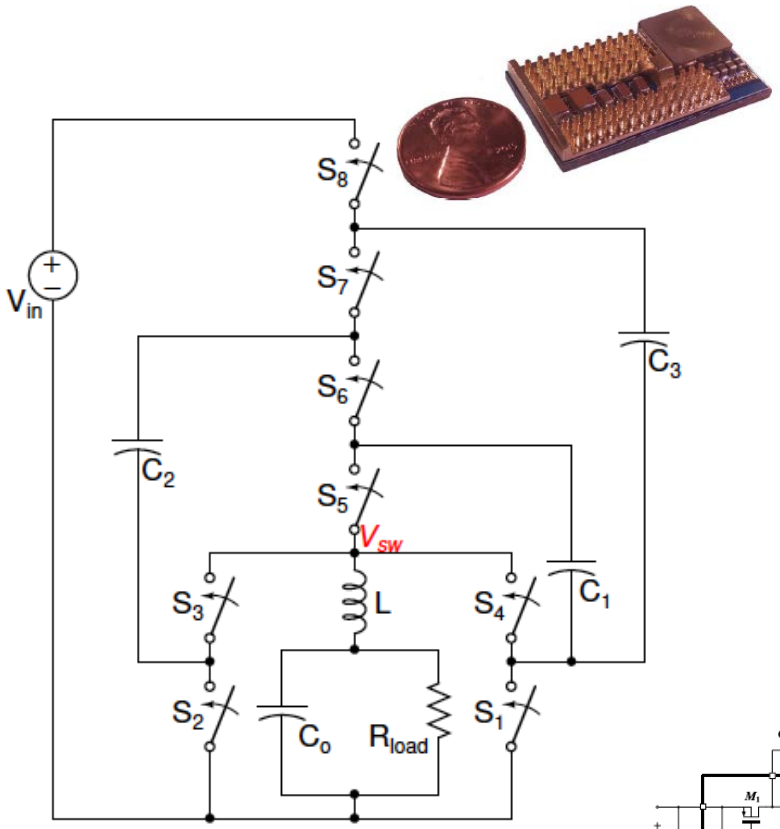
Multitrack PFC power supply

Minjie Chen et al (MIT, Princeton, TI)



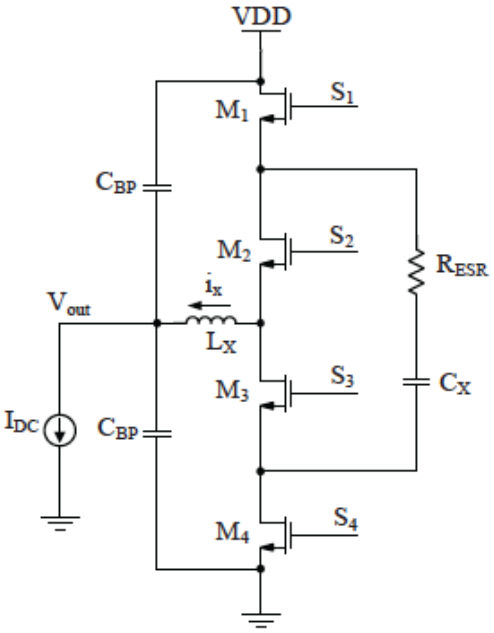
***M. Chen, et al* "Multitrack Power Factor Correction Architecture," *IEEE Transactions on Power Electronics*, (to appear).**

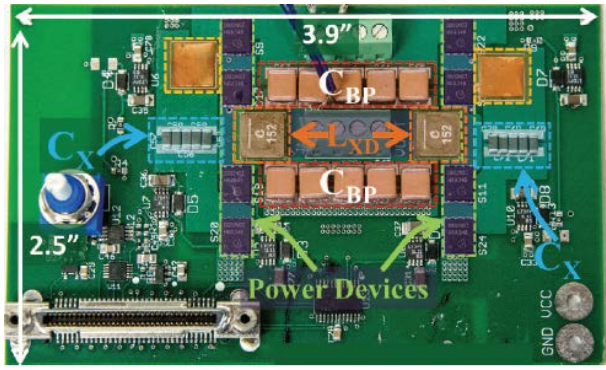
Hybrid SC/Magnetic Conversion



Lei and Pilawa

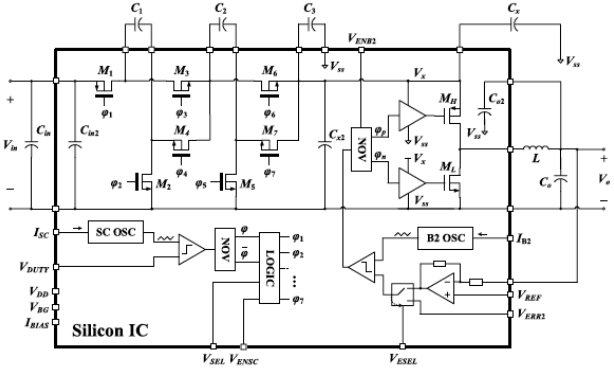
UIUC (ECCE15)

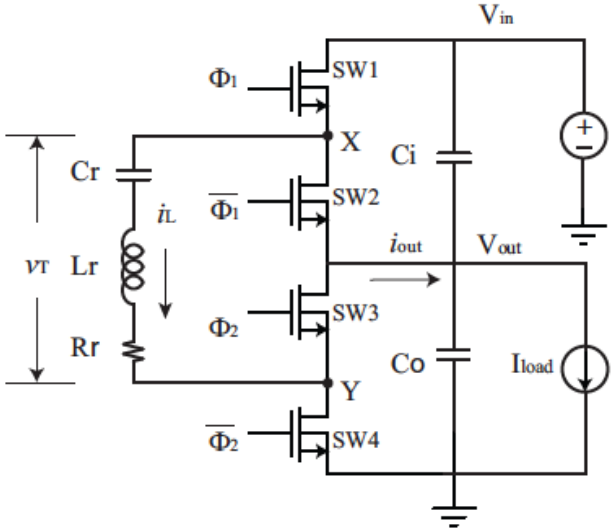




Kesarwani and Stauth

Dartmouth (COMPEL 16)





Sanders et al

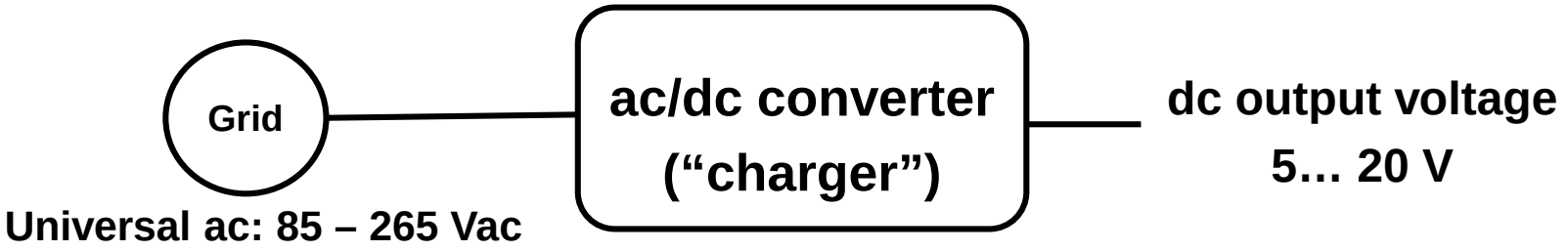
UC Berkeley (COMPEL 15)

Giuliano et al MIT (JESTPE 14)

Hybrid conversion techniques are developing quickly and are advantageous

Example: High Step-Down, Variable-Output Conversion

- **High step-down conversion is a requirement in many applications, such as chargers for portable devices**
  - **Typically interface relatively high universal ac grid input (380 Vpk) to (relatively low) 5 … 20 V dc load**

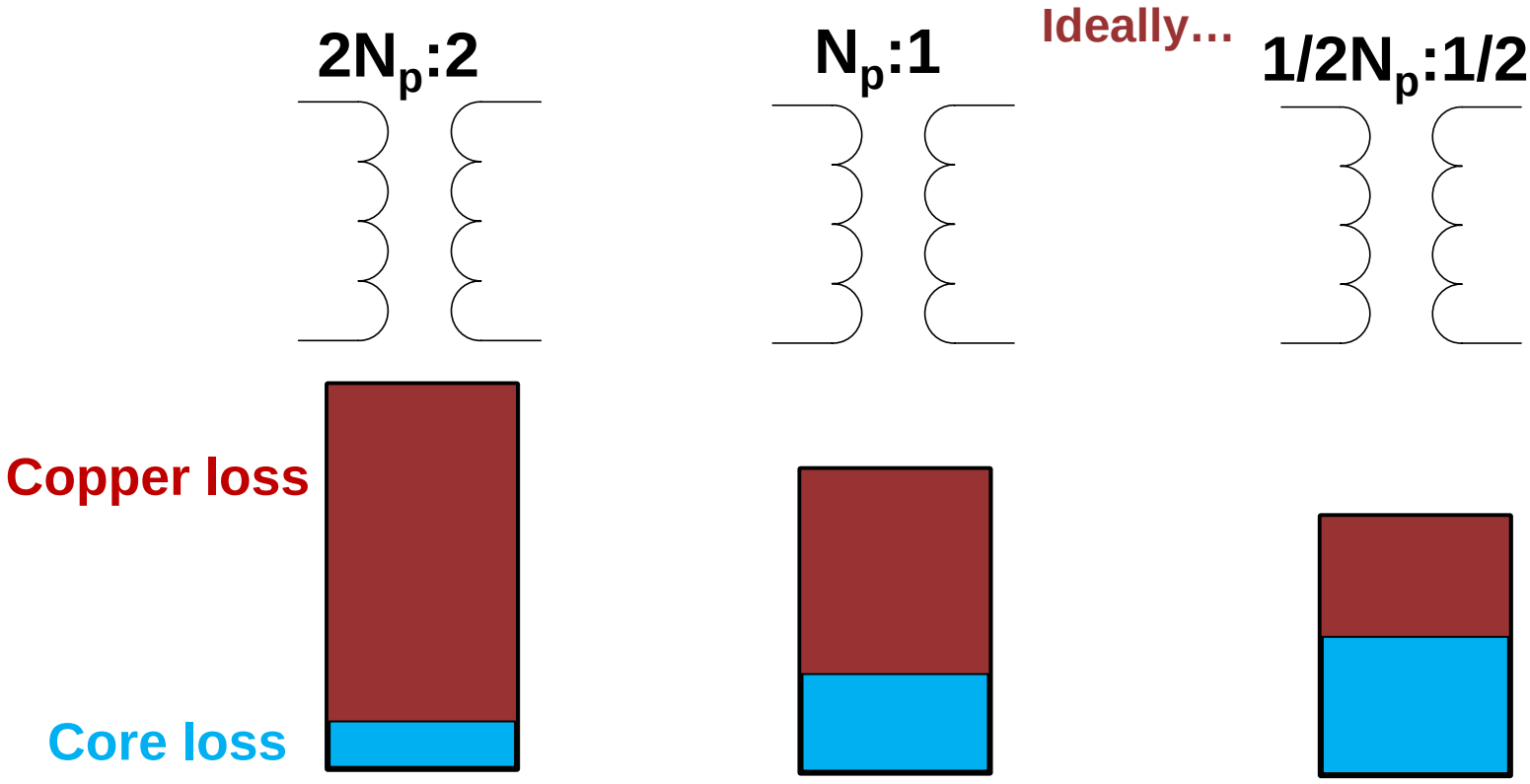


- **Chargers typically have fixed output of 5 … 20 V**
- **Growing interest in chargers that can accommodate *any* of these output voltages**

Challenges to wide-range, large step-down

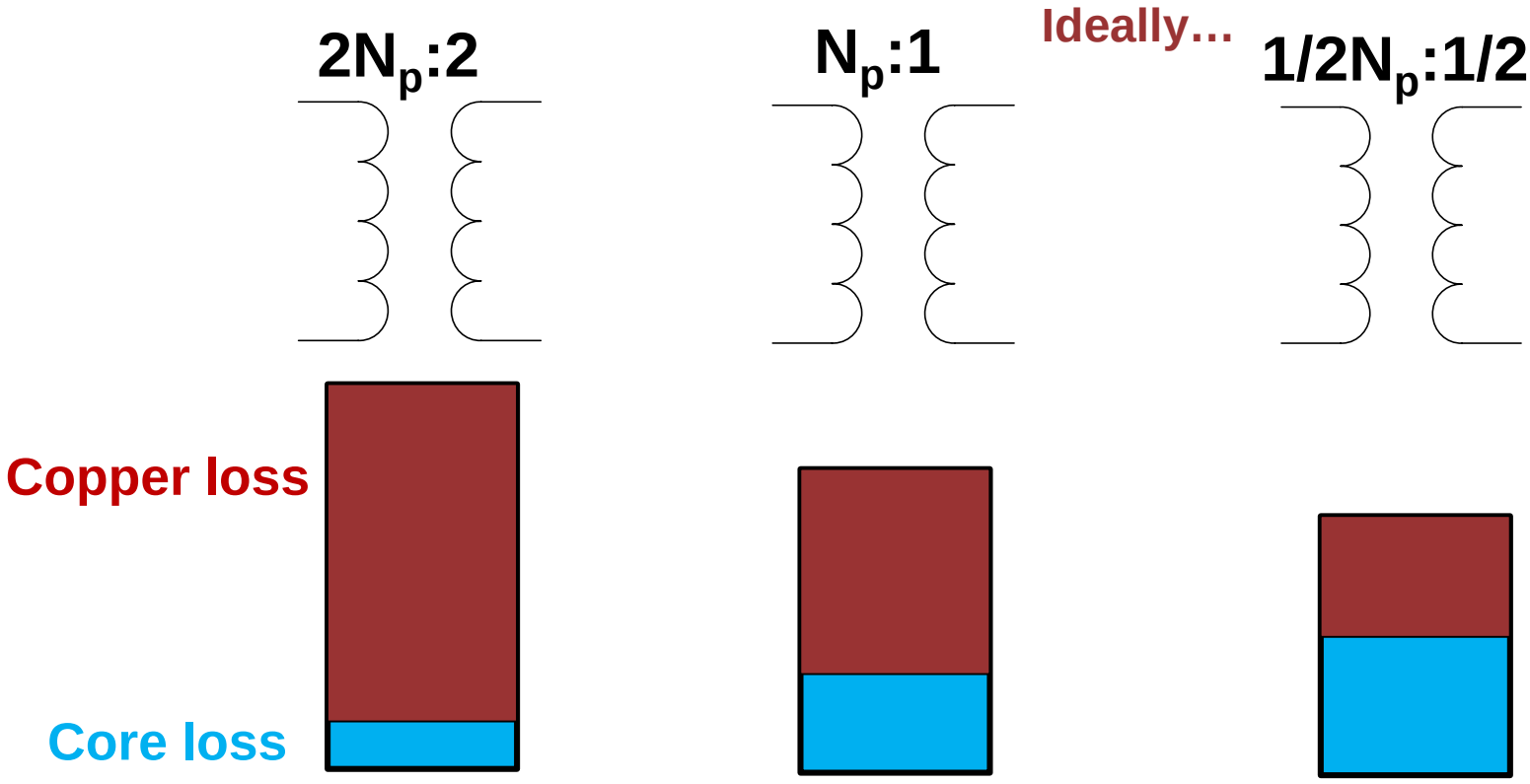
- **Conventional designs often require large step-down ratio transformers**
- **Such transformers are often highly sub-optimal**
  - **Conduction-loss dominated with poor efficiency**
  - **Feasibility: Large number of primary turns (difficult especially if one would like an integrated "planar" transformer)**
- **The wide desired output voltage range also imposes challenges in well-utilizing the transformer**
- **Size and efficiency penalty for the system**
- **More sophisticated transformer / rectifier designs can address both of these problems**

Minimizing Transformer Loss by Turns Selection



- **In transformer design, absolute numbers of turns can be adjusted (while maintaining turns ratio) to minimize loss**
  - **Loss optimized near where core loss and copper loss balanced**
  - **We are often limited by a minimum single secondary turn!**

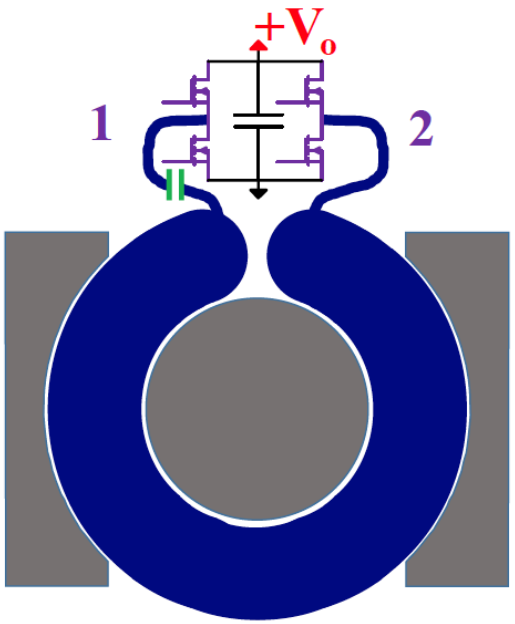
Minimizing Transformer Loss by Turns Selection



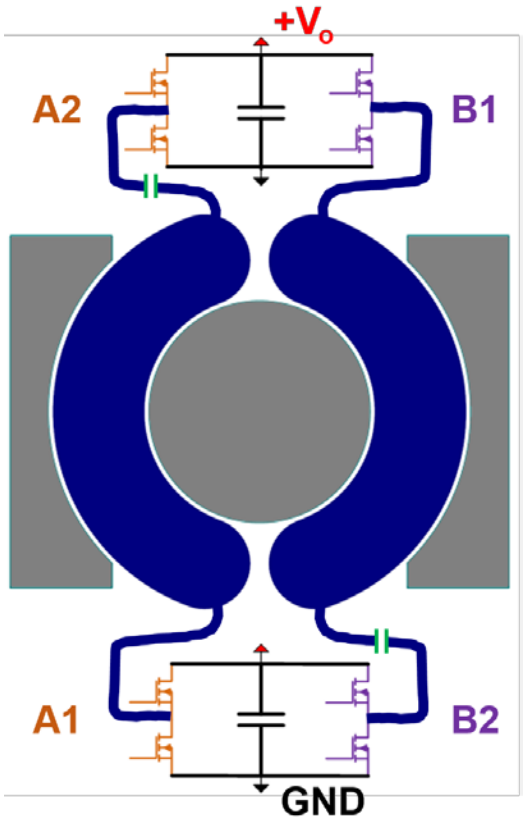
- **How can we realize a "fractional turn" secondary to minimize total loss?**

Integrate Rectifier Operation with Inverter

Single-turn secondary with full bridge rectifier



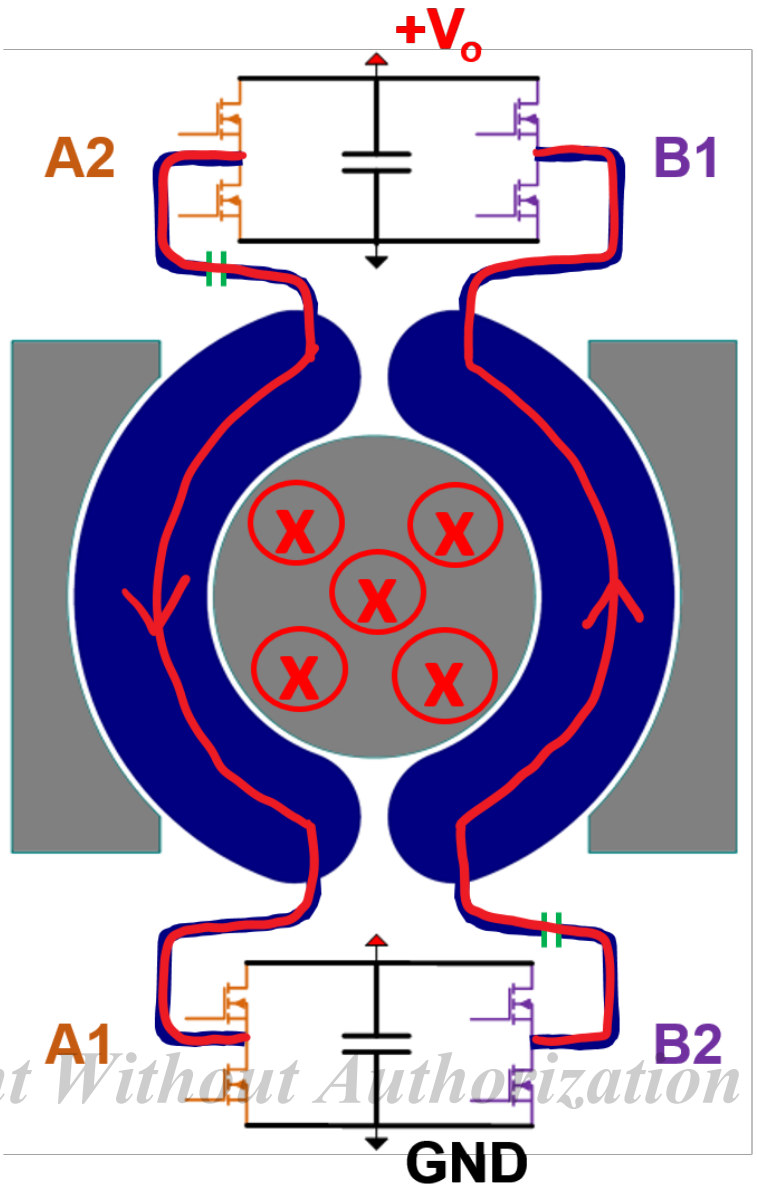
Fractional turns with distributed full-bridge rectifiers: "VIRT"



- **By utilizing more rectifier blocks distributed around the core, we can gain effective fractional turns!**
  - **Termed a "Variable Inverter-Rectifier-Transformer", or "VIRT"**

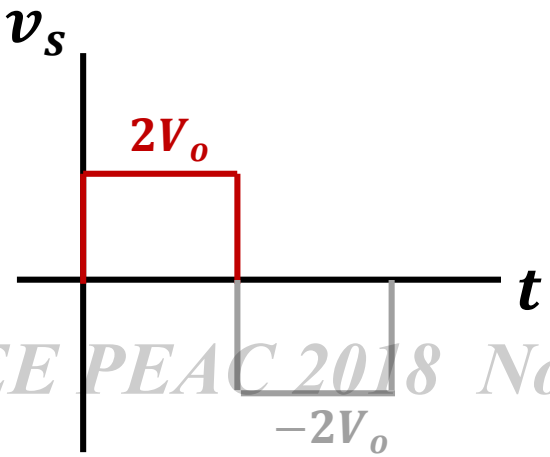
VIRT: Principle of Operation

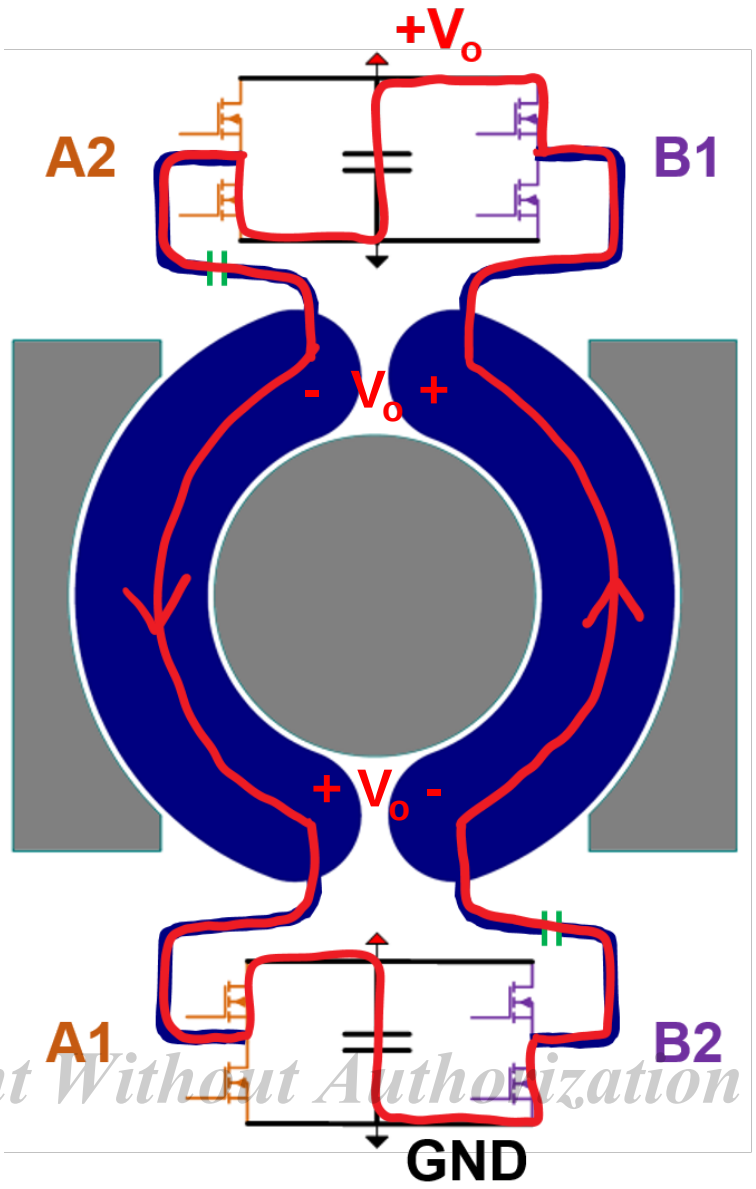
- N_p primary turns are wound on the center post (not shown)
- ac voltage applied to primary drives flux through the center post
- How the centerpost flux links each of the "fractional" turns is determined by the switching operation of the distributed rectifiers



VIRT: Principle of Operation

- For symmetric operation of the distributed rectifiers as full bridges (“FB/FB”), each “half-turn” links half the flux
- Dc output voltage is inserted into the ac flux loop twice
  - Vp/Np = 2 Vo
- We get two effective (Np/2):(1/2) transformers!





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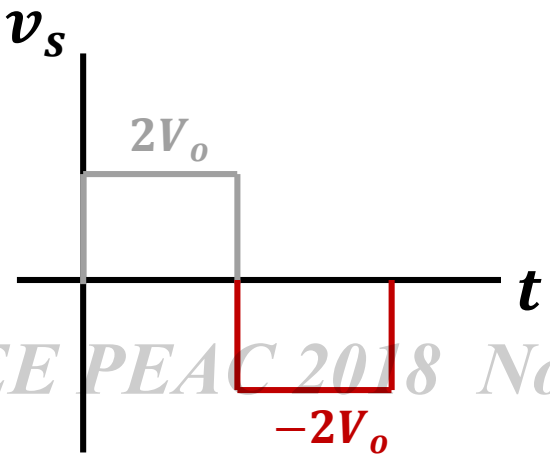
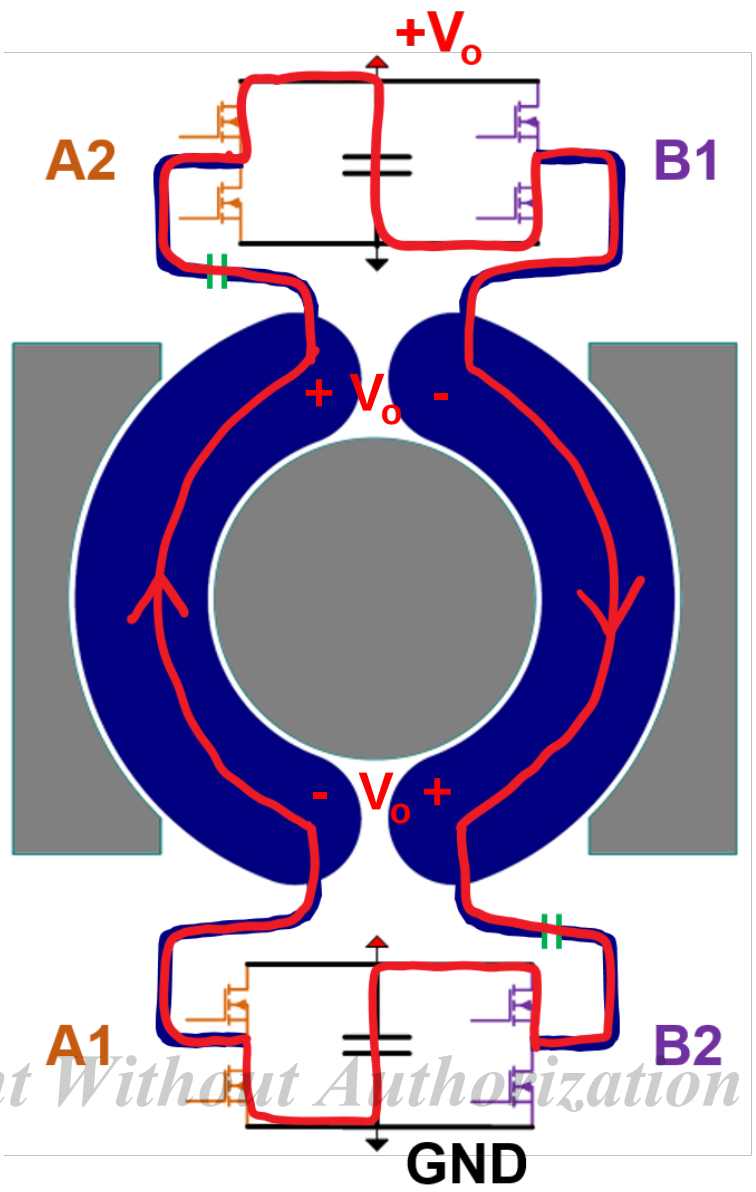
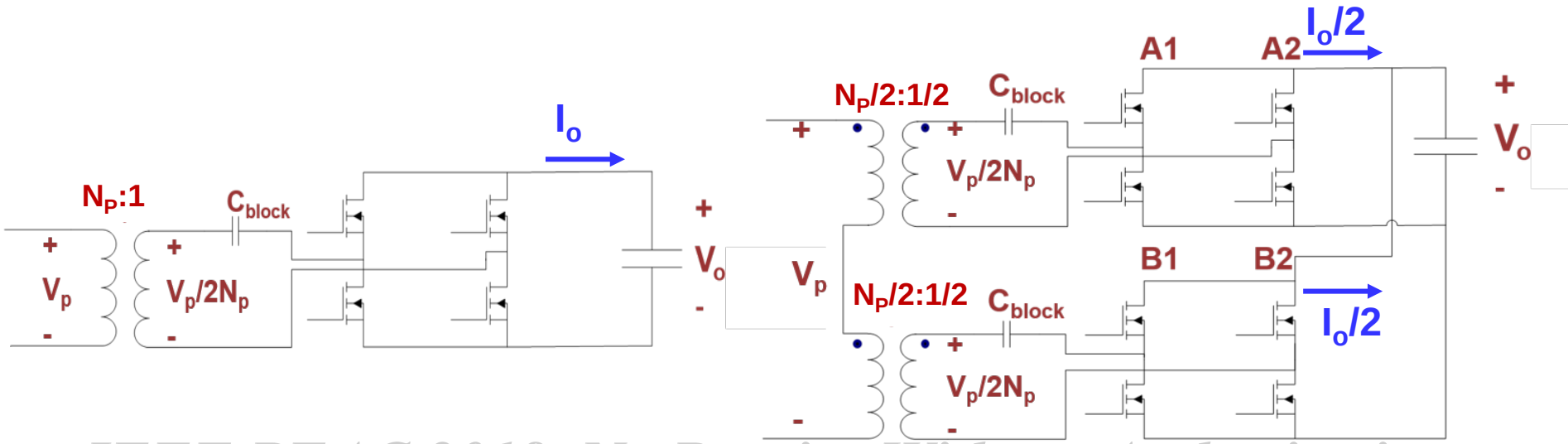




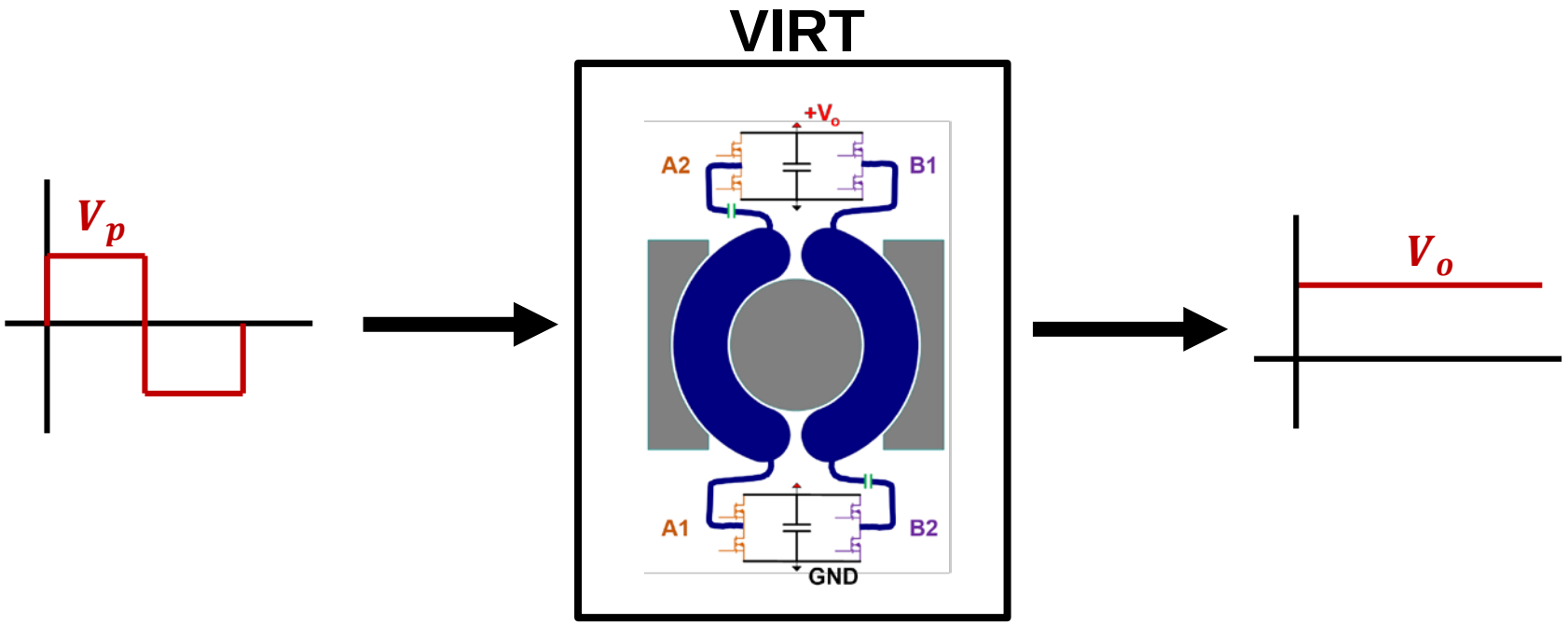
Identical Switch Loss for Same Transistor Area

- **Although VIRT requires 2x the switches, each switch carries 1/2x the current (re the conventional case)**
  - **Identical die area for the same loss and power transfer**

Conventional FB	VIRT
$P_{cond} = 2\frac{R_{on}}{2} I_o^2 = R_{on} I_o^2$	$P_{cond} = 4R_{on}\left(\frac{I_o}{2}\right)^2 = R_{on} I_o^2$

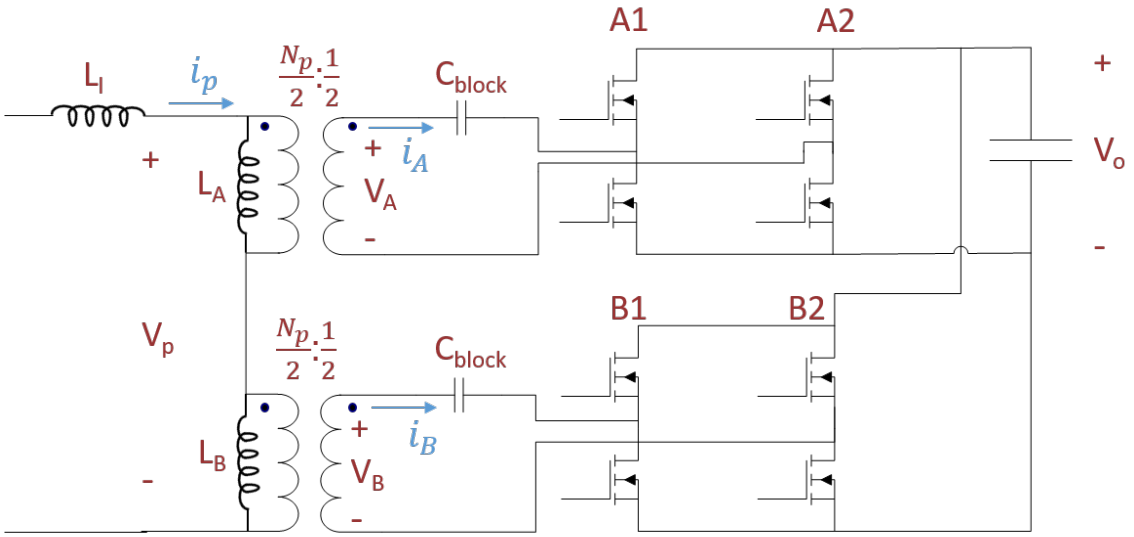


VIRT: Variable Inverter Rectifier Transformer



- **We now have multiple rectifiers. We can operate each rectifier set in *different* modes (switching patterns)**
  - **Full Bridge (FB), Half Bridge (HB), Zero (0)**
- **We can use this to realize *four different* conversion ratios from the ac primary voltage to dc output voltage**

VIRT Electrical Model

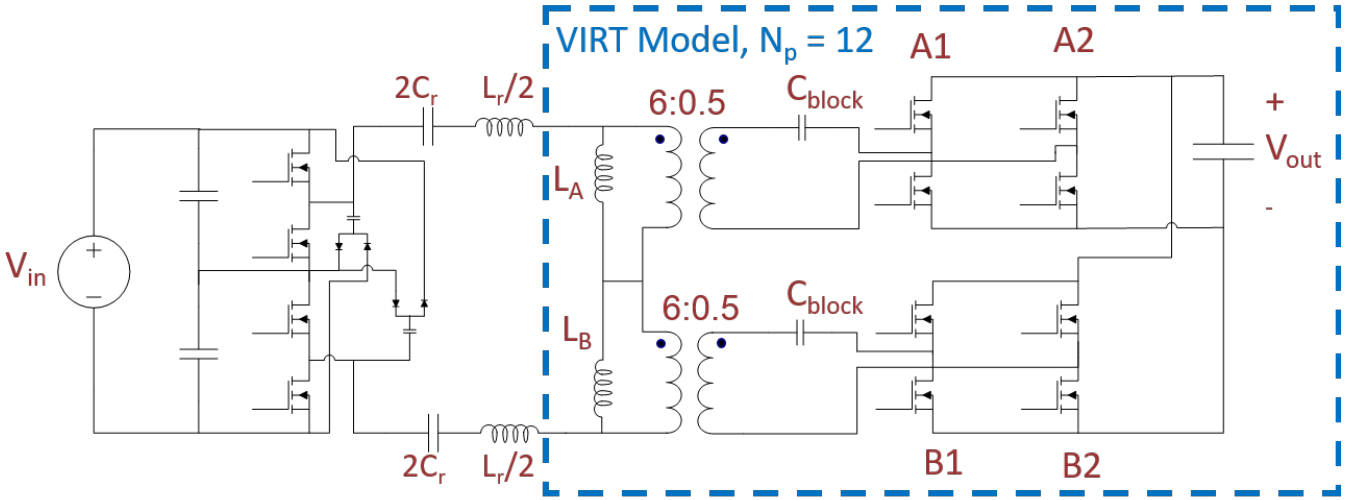


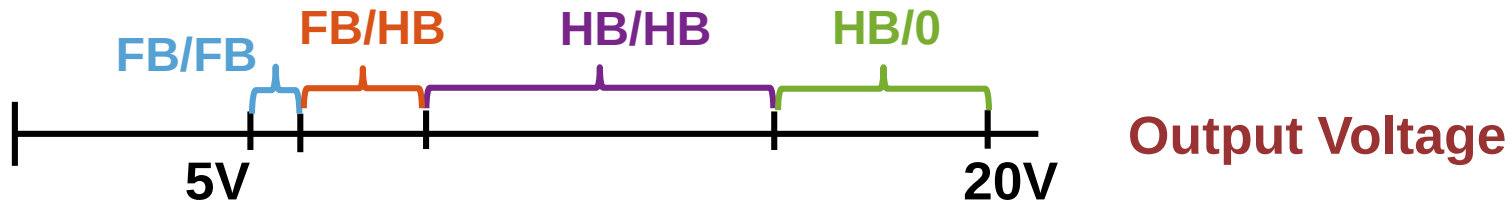
Mode	Switching pattern	Output voltage	Vp:Vo conversion ratio
FB/FB	• All switches active	$V_o = V_p \frac{1/2}{N_p}$	$N_p:\frac{1}{2}$ (x4/3)
FB/HB	• B2 held in low state • A1, A2, B1 active	$V_o = V_p \frac{2/3}{N_p}$	$N_p:\frac{2}{3}$ (x4/3); x2
HB/HB	• A2, B2 held in low state • A1, B1 active	$V_o = V_p \frac{1}{N_p}$	$N_p:1$ (x2); x4
HB/0	• A2, B1, B2 held in low state • A1 active	$V_o = V_p \frac{2}{N_p}$	$N_p:2$ (x4)

- ***Fractional turns* and *reconfigurable conversion ratio*!**

Prototype Stacked-Bridge LLC+VIRT Converter

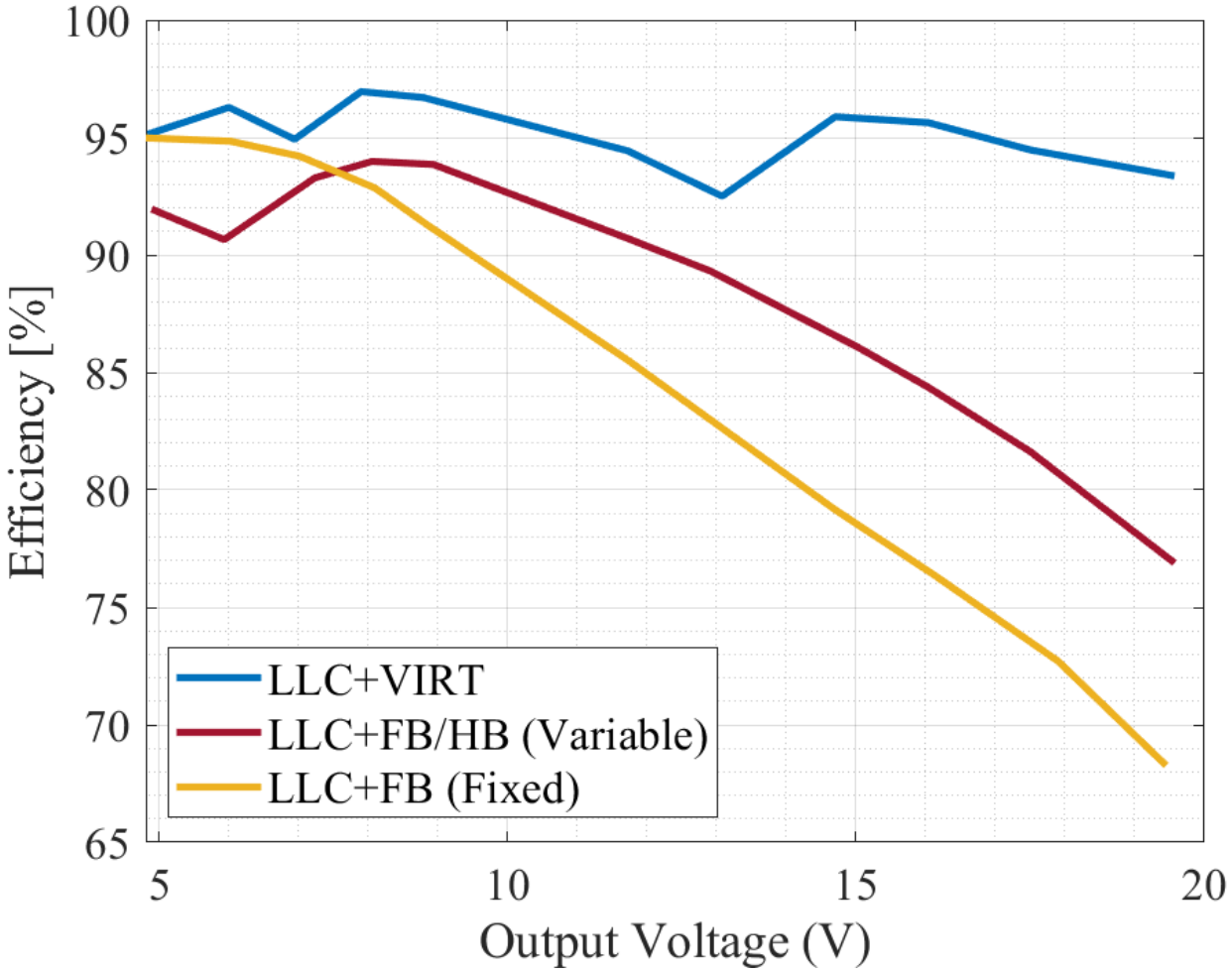
- **Stacked-bridge LLC: 120-380 Vdc input to 5 – 20 Vdc output (5A/36W)**
- **VIRT transformer/rectifier provides "fractional" turns and compresses output voltage range**





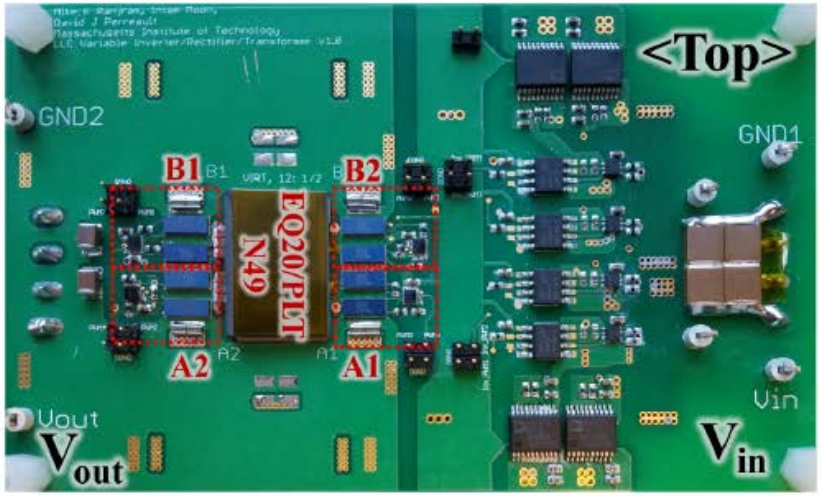
M.K. Ranjram, et al, "Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure…" *IEEE Transactions on Power Electronics,* 2018

Simulated Performance (with and without VIRT)

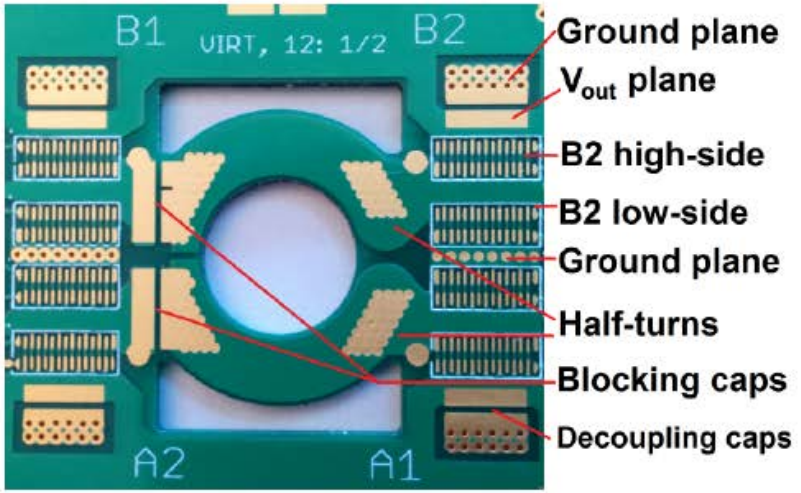


- **Simulated converter performance across output voltage**
  - **Designs with and without mode changes and VIRT**
  - **for Vin=190 V, Iout = 5 A (@ <7.2 Vout), Pout = 36 W (@> 7.2 Vout)**

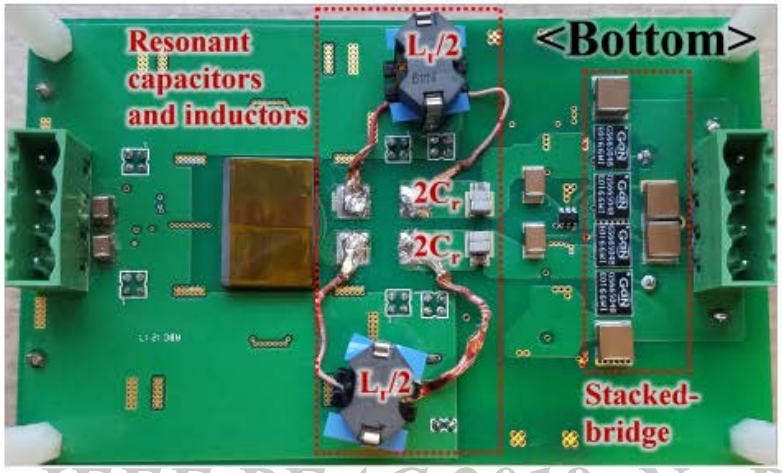
VIRT Prototype Implementation



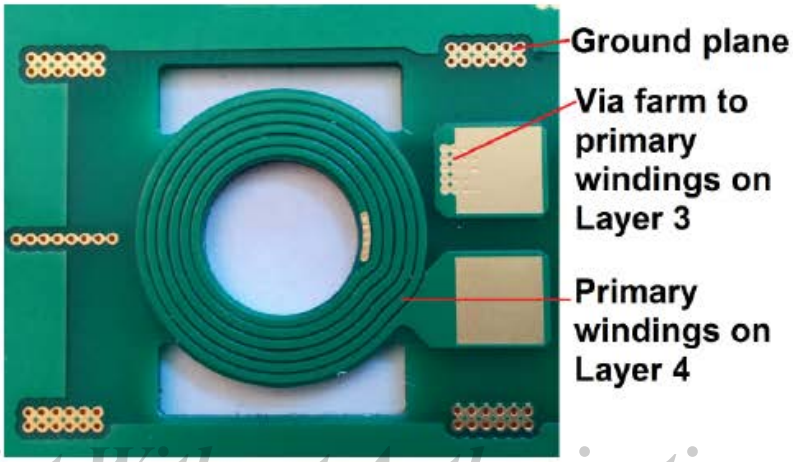
(a) Top side



(b) Top side, VIRT layout



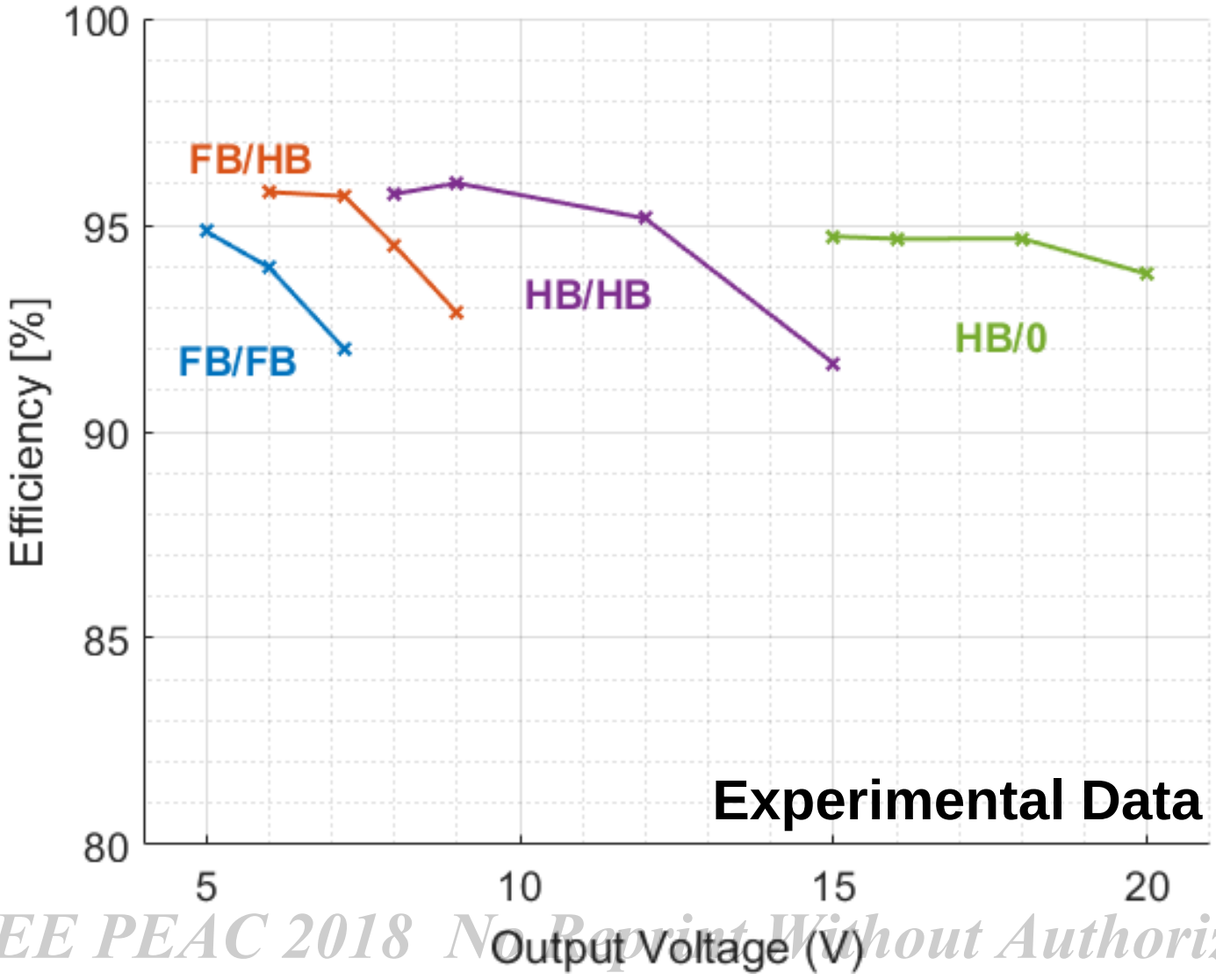
(c) Bottom side



(d) Bottom side, VIRT layout

M.K. Ranjram, et al, "Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure…" *IEEE Transactions on Power Electronics*, 2018

VIRT Enables High Efficiency Over Wide V_{out}



Summary (1)

- **Magnetics scaling poses *fundamental* challenges in power electronics design**
- **Improvements in semiconductor devices, integrated circuits / controls, magnetic materials, and packaging open the door to greatly improved power electronics**
- **Substantial improvements in size and performance of power electronics are possible through more sophisticated designs that *judiciously* leverage complexity**
- **Two examples:**
  - **Multitrack conversion (dc/dc and ac/dc PFC)**
  - **VIRT**

Summary (2)

- **There is tremendous room for innovation and performance improvement with such techniques**
  - **Architectures and topologies (including designs enabling HF)**
  - **Improved passives, packaging and integration**
  - **Better utilization of new semiconductor devices and controls**

- **Acknowledgements**
  - **MIT Power Electronics Research Group**
  - **Sponsors: Texas Instruments, NSF, ARPA-E, MIT CICS, Futurewei, …**

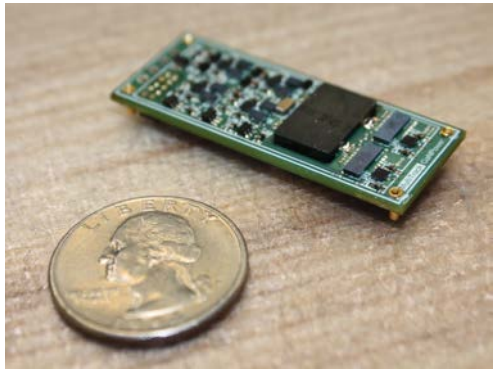
THANK YOU!

Challenges

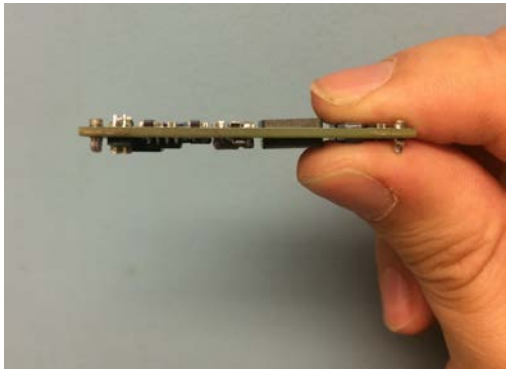
- **Even at constant or improved total VA ratings of power devices, increased component counts (including controls, level shifters, drivers,…) can increase cost**
  - **Modularity, integration, and improved passives and thermals can help mitigate this**
  - **Better size, efficiency and performance can justify it**
- **More sophisticated designs require greater engineering design effort (*at least the first time…*)**
  - **Validate performance and reliability across operating modes, manage mode transitions, more sophisticated startup requirements, more potential fault modes…**
  - ***Requires more sophisticated designers!***
- **Approaches provide the biggest *initial* benefit in:**
  - **High-performance applications**
  - **High-volume applications**

18V-80V, 75W Miniaturized Telecom Converter

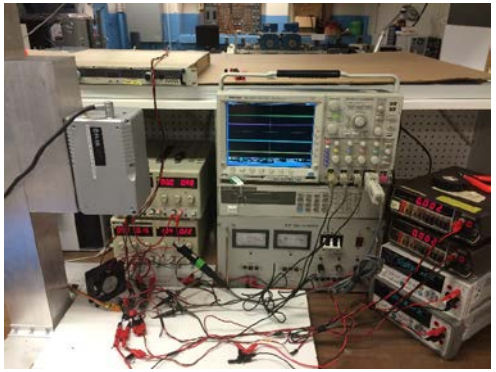
Small Volume



Light Weight



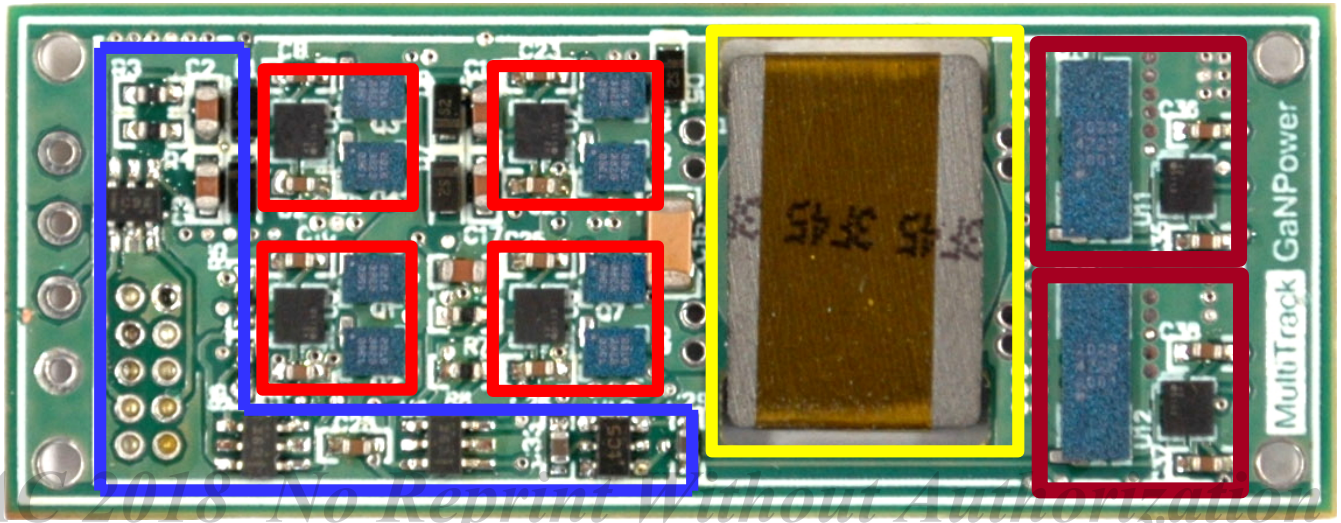
High Efficiency



Modular Input Cells **PCB Integrated Transformer** **Modular Output Cells**

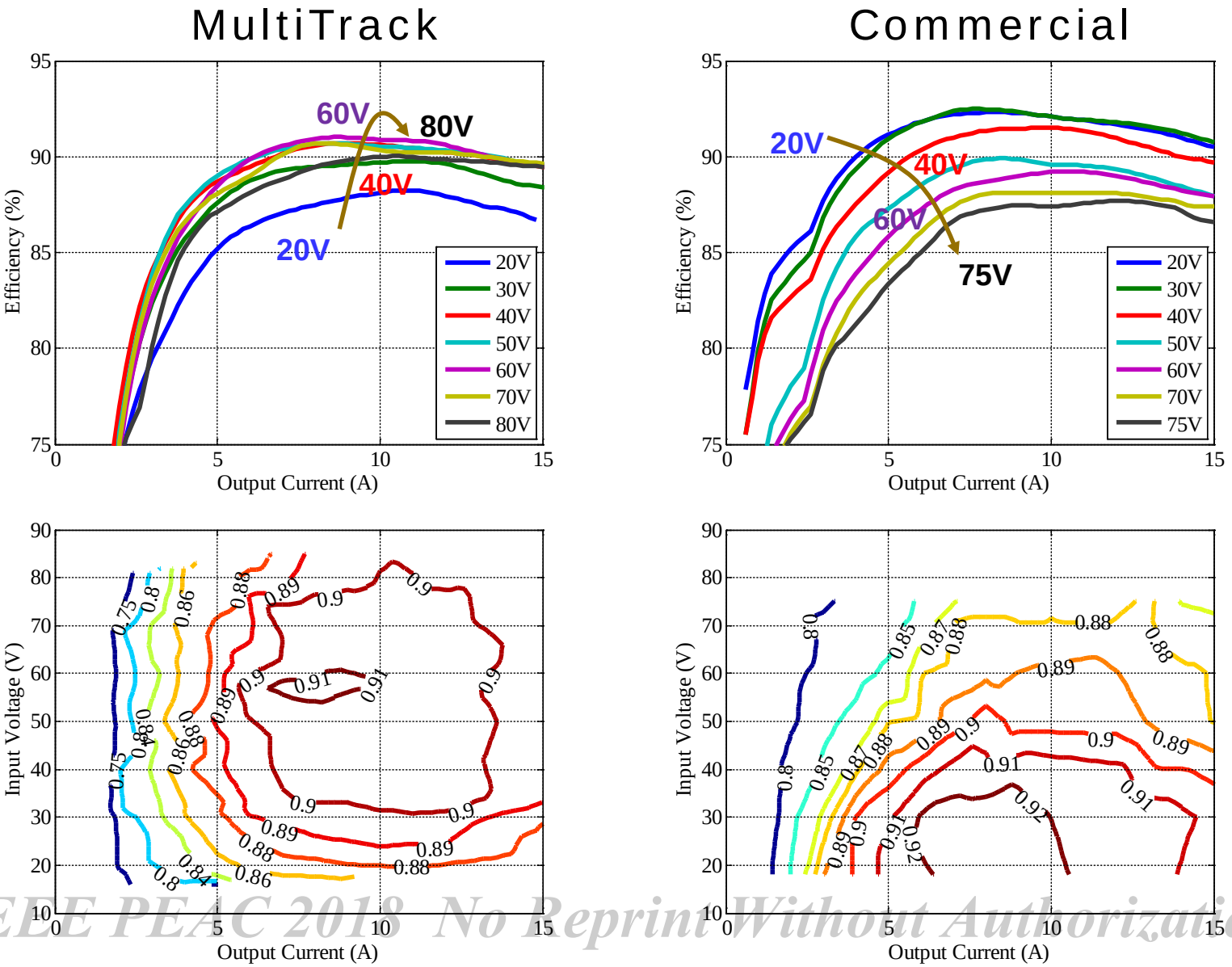
8 Layer PCB with precisely controlled parasitics

Discrete Logic, LDOs, Controls, Signal Buffers, …



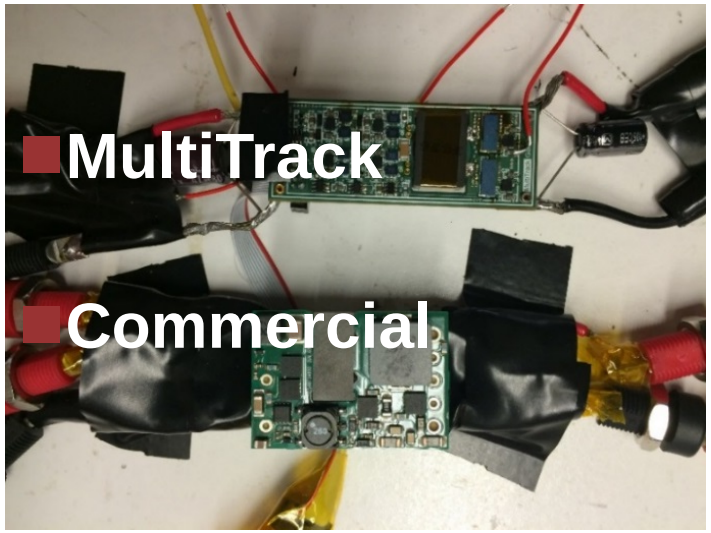
GaN Switches (from EPC) + Drivers for GaN (from Texas Instruments)

Efficiency vs. Operating Point

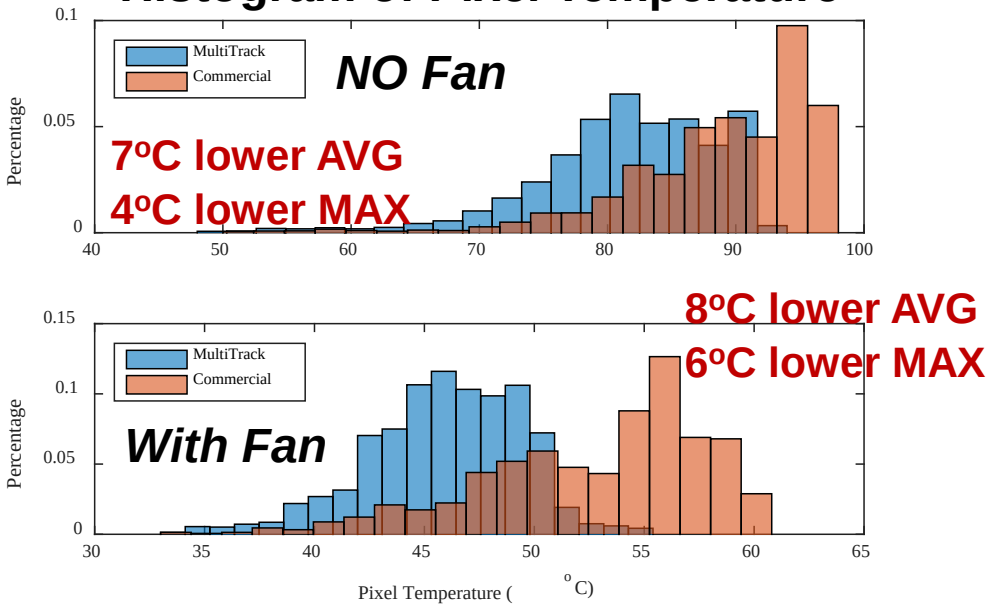


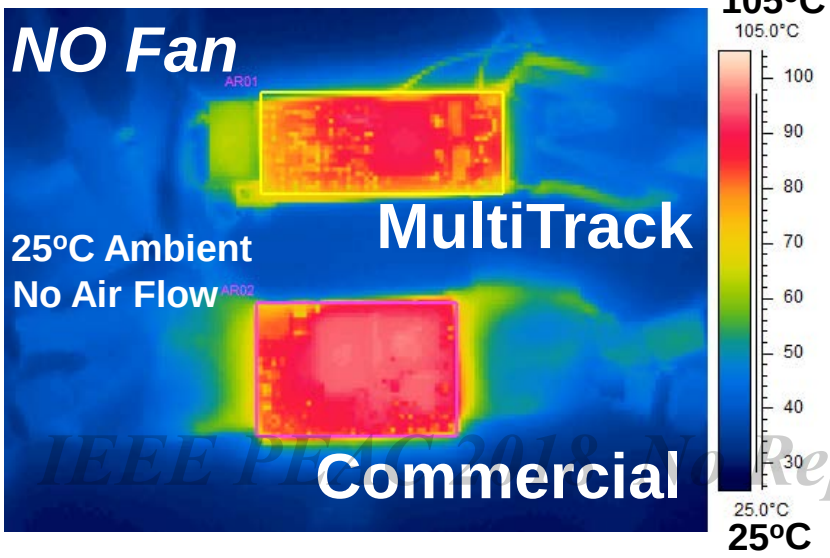
Lower Cooling Requirements

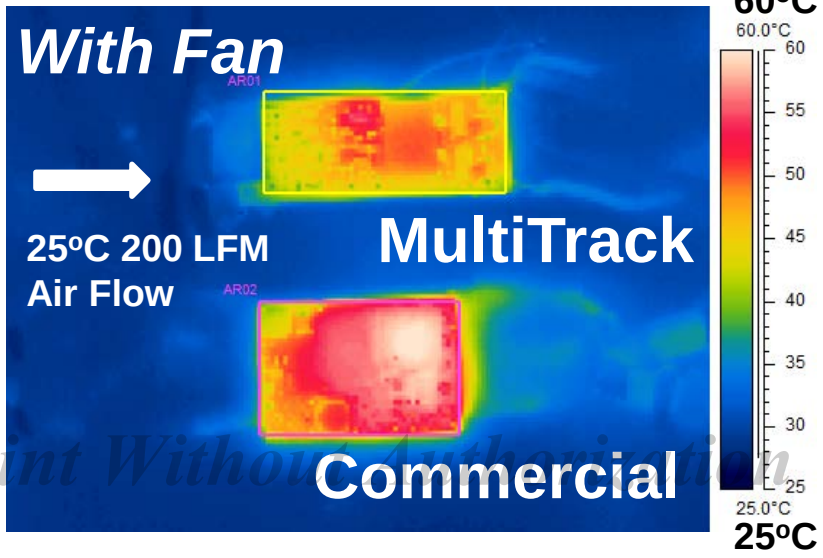
41.3 V_{in}, 5 V_{out}, 7 A_{out}, ~90% Efficiency



Histogram of Pixel Temperature

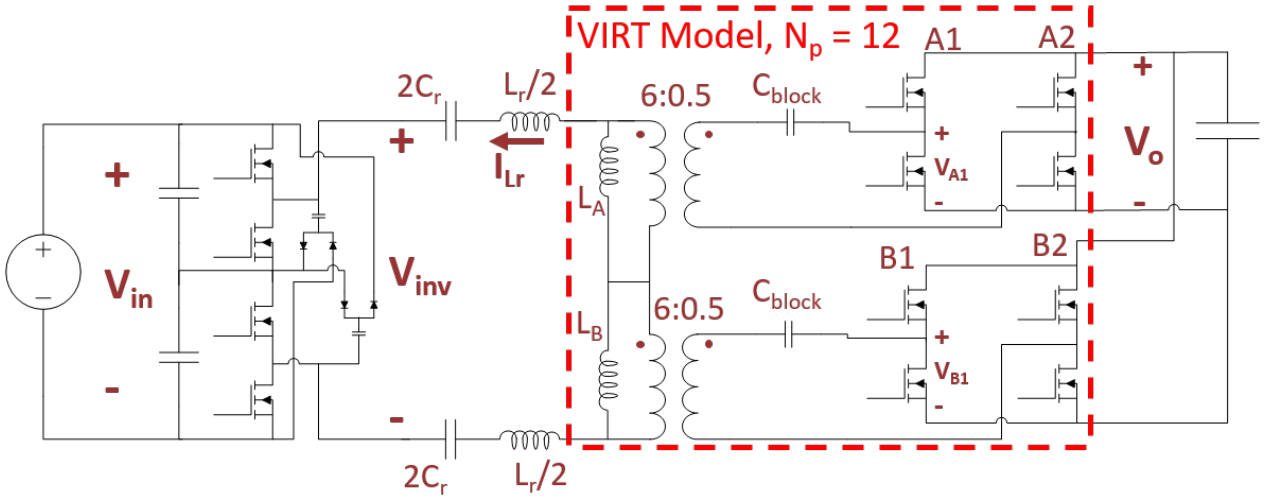




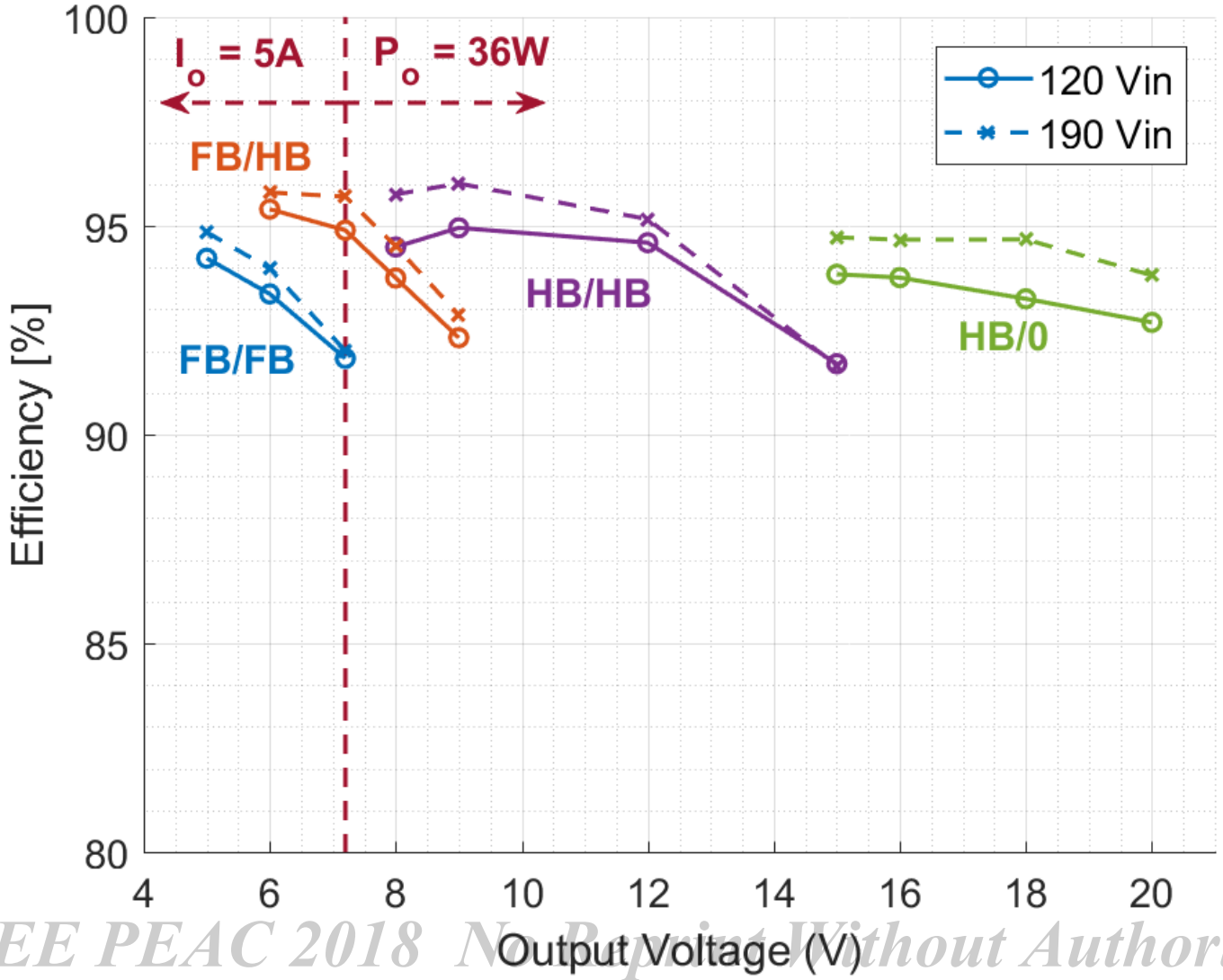


Prototype Stacked-Bridge LLC+VIRT Converter

- **A 120-380 Vdc input to 5 – 20 Vdc output (5A/36W) experimental prototype is presented**
- **VIRT compresses output voltage**
- **Additional converter gain blocks (stacked-bridge and LLC) are used to interpolate output voltage**

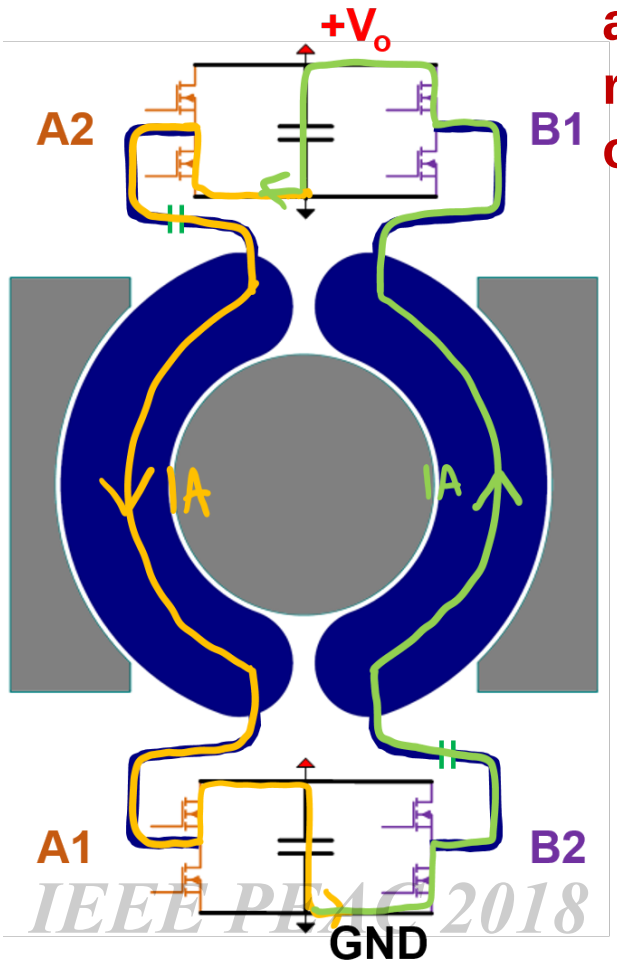


VIRT Benefit for Efficiency is Clear

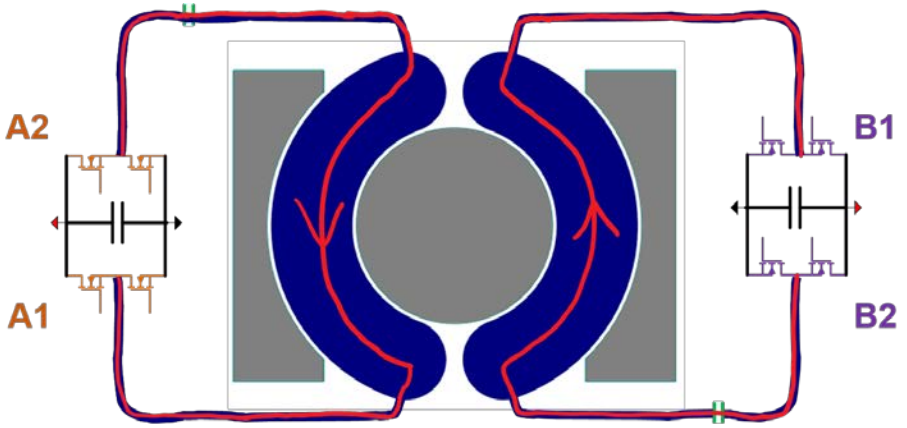


VIRT vs. "Conventional" Alternative

- **In VIRT, there exists another path for rectifier current to return and this return path is shorter than in the "conventional" alternative**

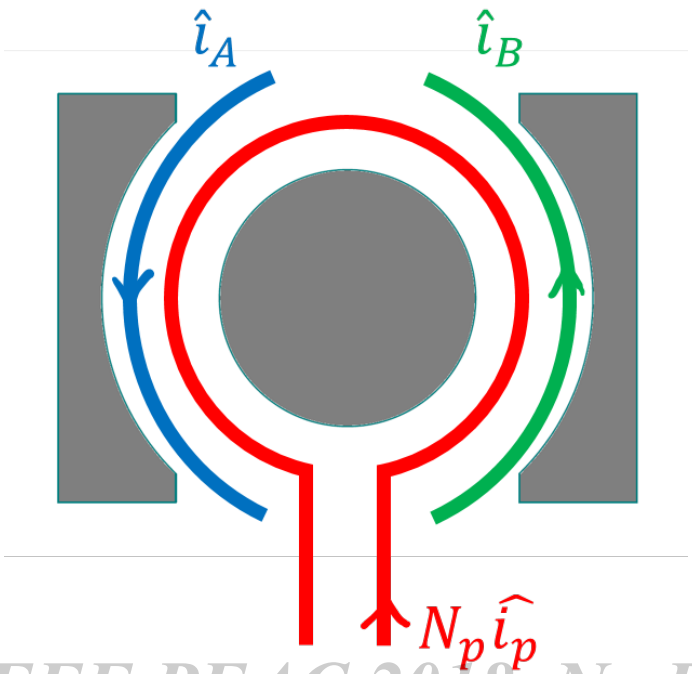


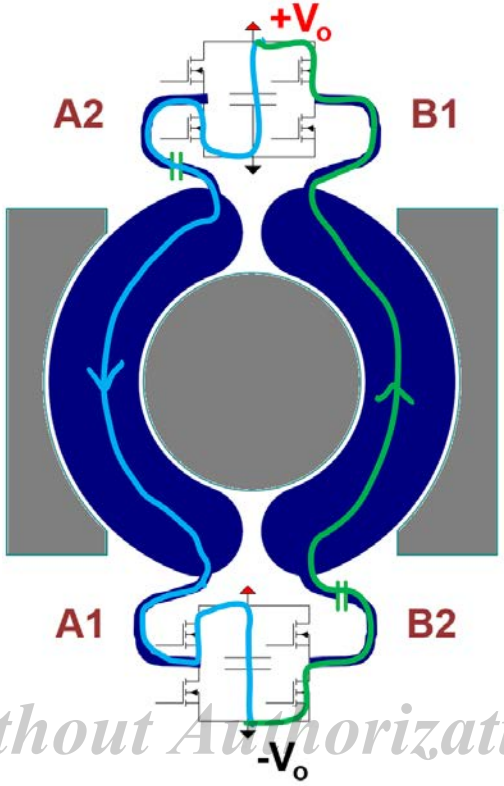
ac current can return through the other half-turn



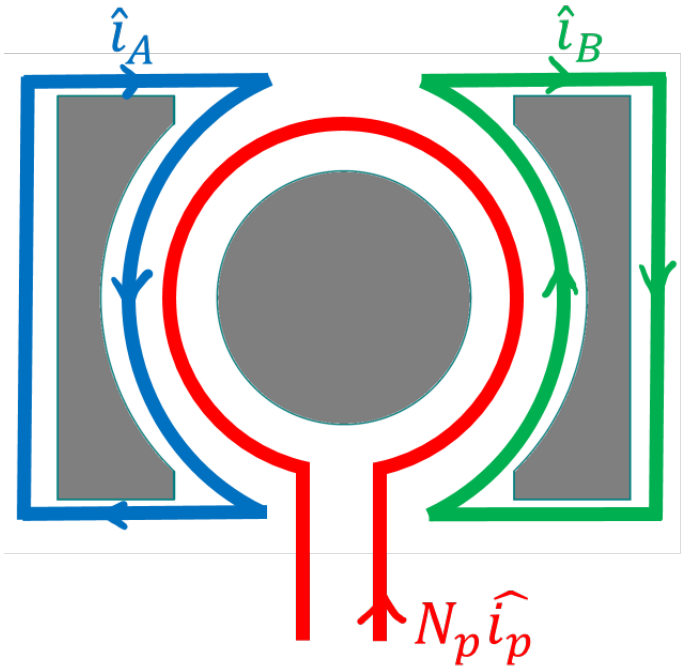
ac current *must* return around the outer core legs

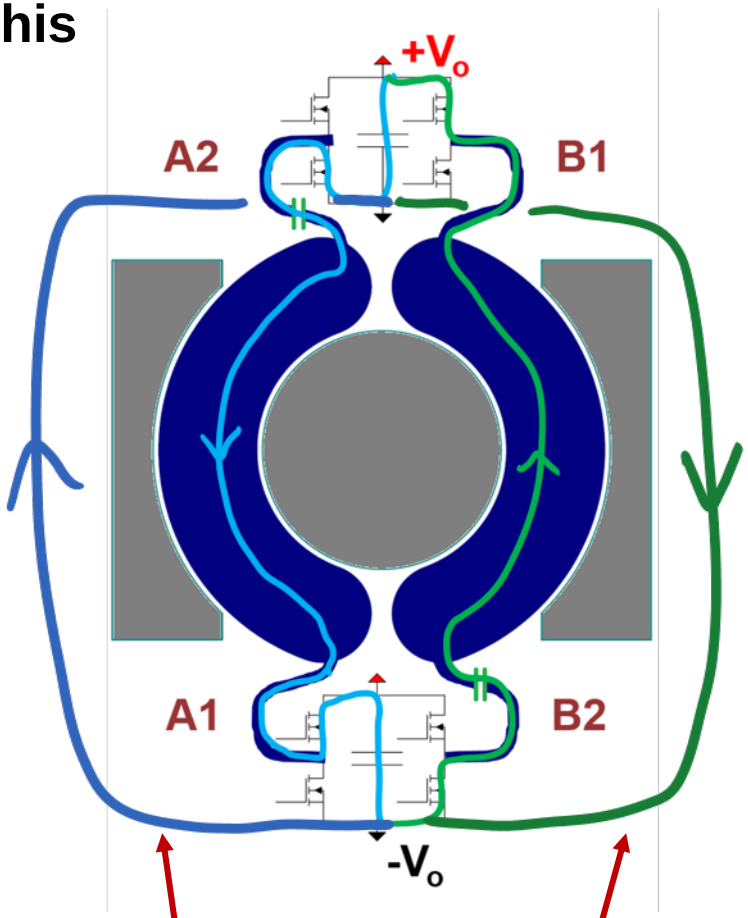
- **Derive magnetic circuit model to create electrical model**
- **Need to describe current flow in system using closed current loops**
  - **Start with the known current flows: primary windings and components of rectifier current inside core**





- **Assume the rectifier currents return outside the core for modeling purposes *only***
  - **We invoke “virtual currents” to do this**

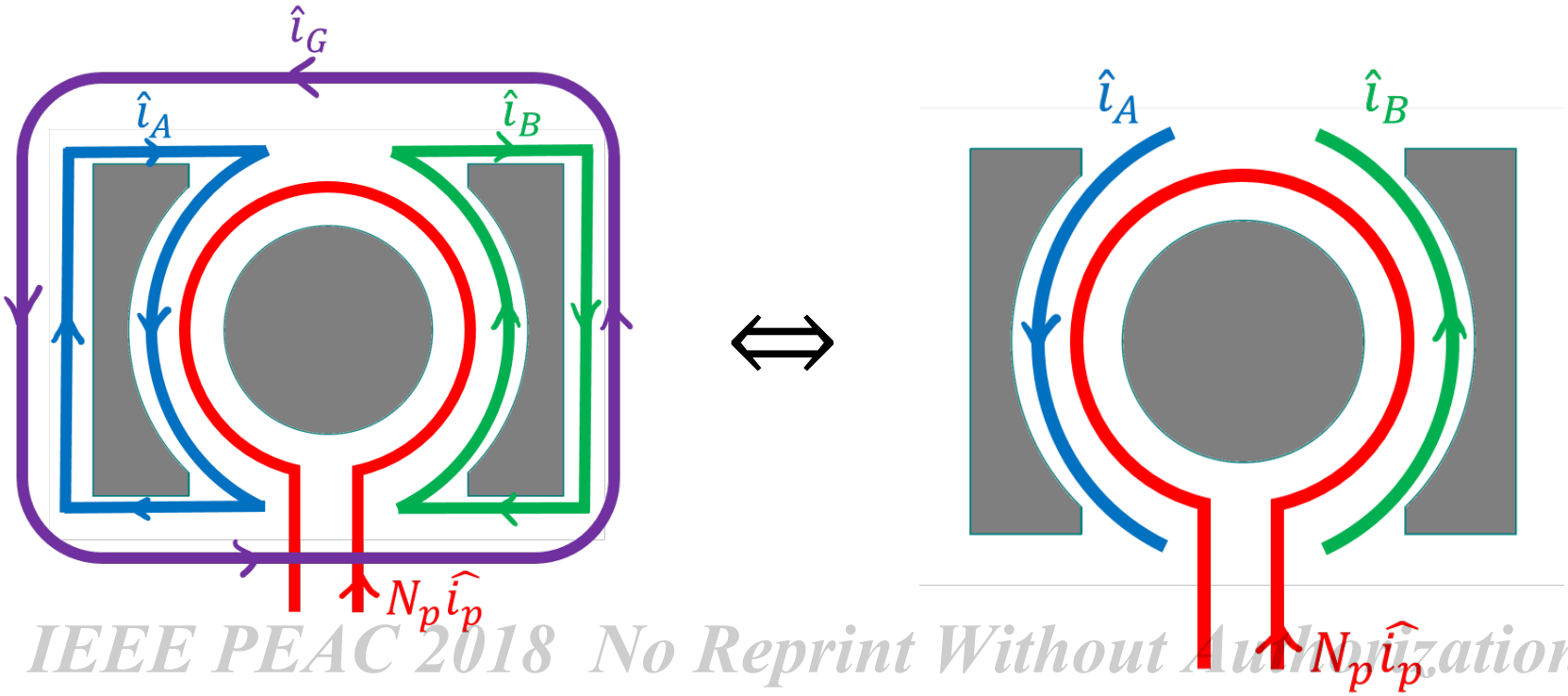




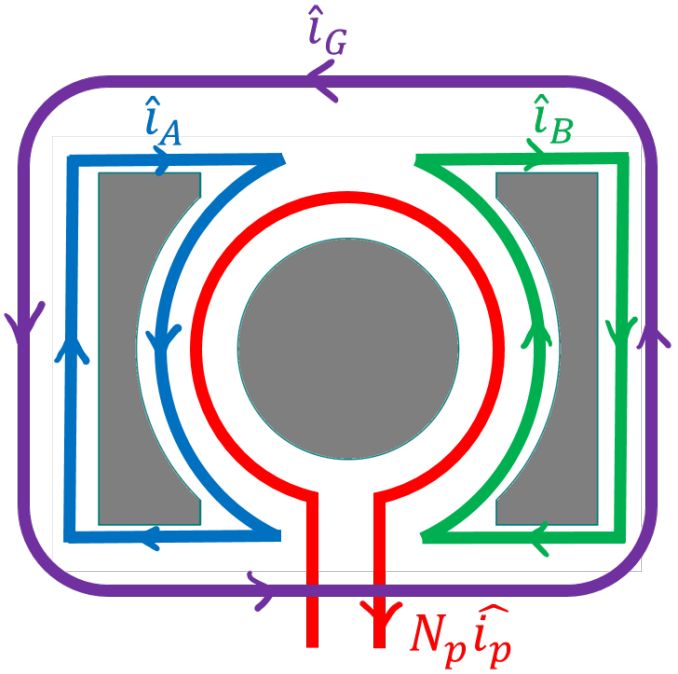
The components of $\hat{i}_A$ and $\hat{i}_B$ that are outside the core are “virtual”

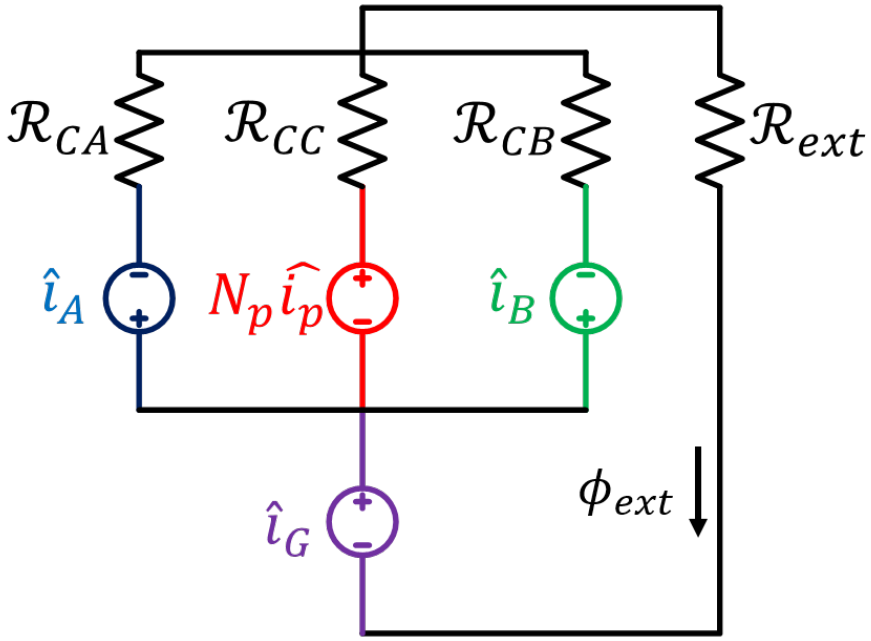
2. Invoke Second Virtual Current

- **To cancel the virtual components of $\hat{\imath}_A$ and $\hat{\imath}_B$ we invoke an additional virtual current $\hat{\imath}_G \cong \hat{\imath}_A \cong \hat{\imath}_B$**
- **Note that if we sum all of these currents, the "virtual" components are nulled and we obtain the original (real-world) current flow**



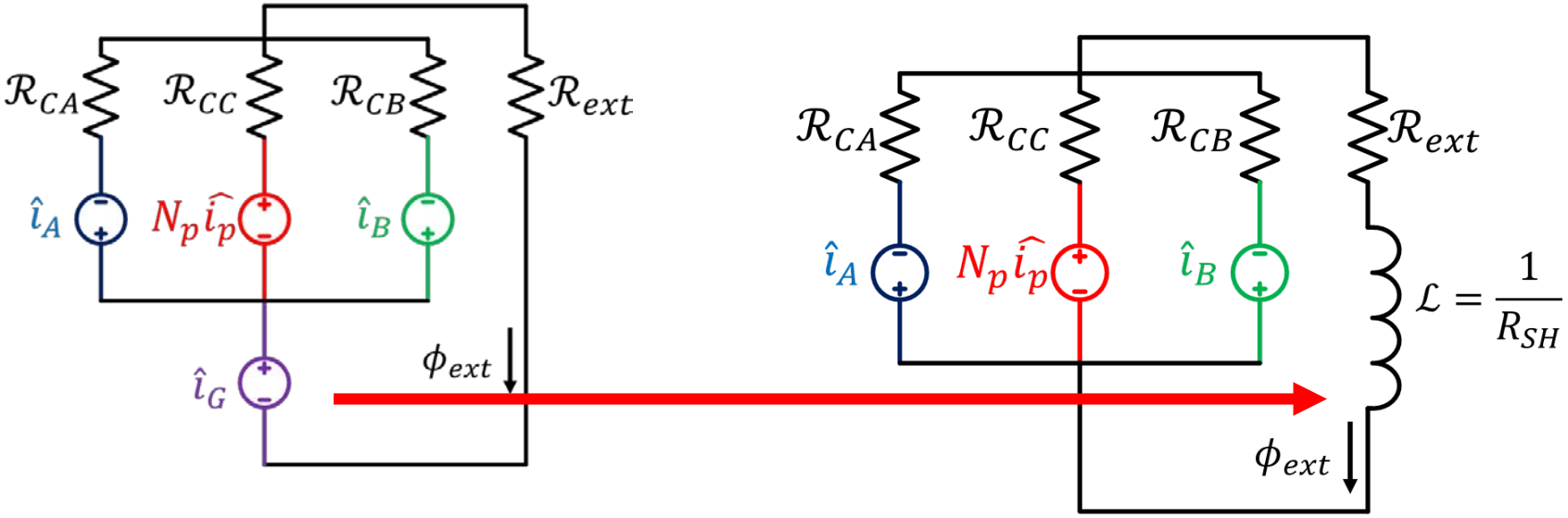
- **With current flow now in closed loops, can create magnetic circuit**





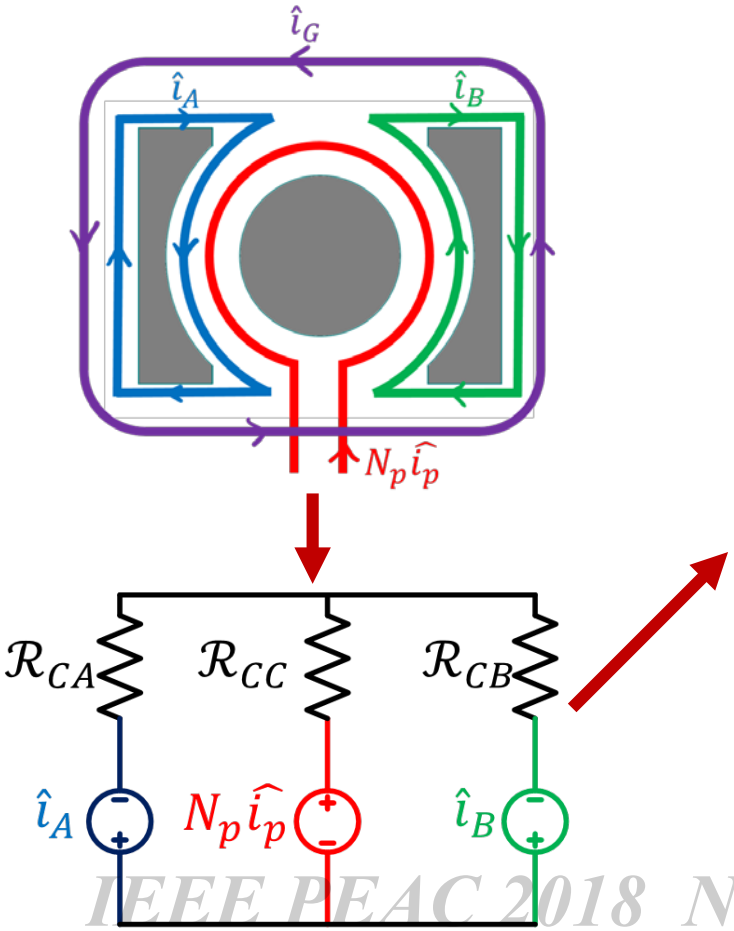
Associate External MMF with Transference Element

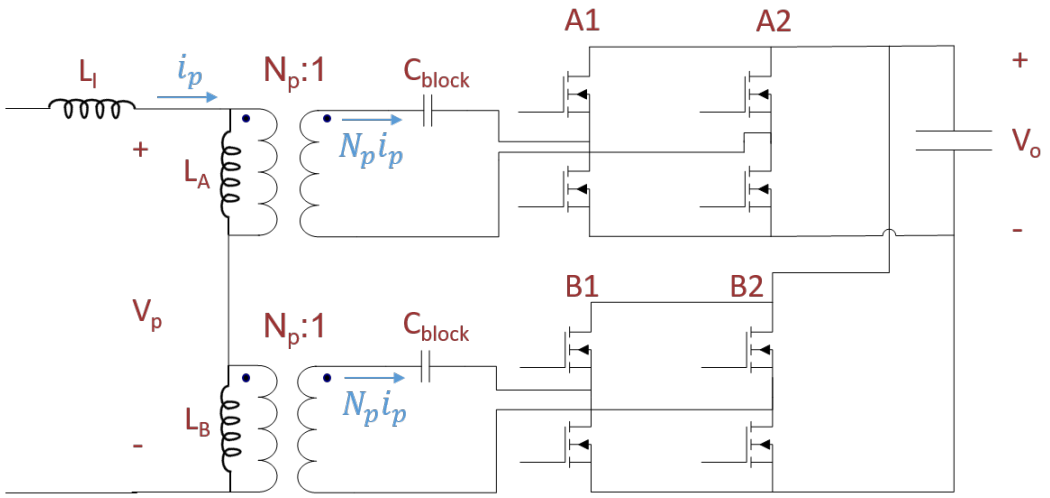
- **With current flow now in closed loops, can create magnetic circuit**
  - **In practice, MMF associated with short-circuit path of $\hat{\imath}_G$ is associated with small induced voltage due to small resistance R_{SH} of ground-plane around core**
  - **Model this using transference element $\mathcal{L}$ [1]**



[1] E. R. Laithewaite, "Magnetic equivalent circuits for electrical machines," Proceedings of the Institution of Electrical Engineers, vol. 114, no. 11, pp. 1805–1809, November 1967.

- **In the ideal case where R_{SH} has zero resistance, and $\mathcal{R}_{CA} = \mathcal{R}_{CB}$ magnetic circuit simplifies and we extract the electrical circuit model**





Symmetric vs. Asymmetric Operation

- **Symmetric Operation: Both rectifiers operated in an identical manner (i.e. FB/FB or HB/HB modes)**

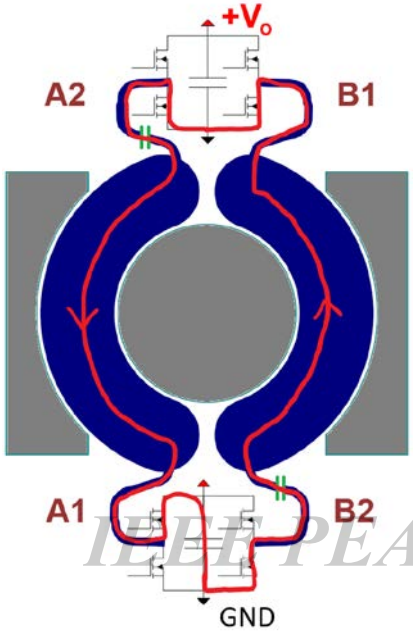
- **Asymmetric Operation: Any other configuration (e.g. FB/0 or HB/0 modes)**

- **Compared to symmetric operation, asymmetric modes have:**
  1. **Worse core utilization (higher core loss for the same voltage)**
  2. **Smaller magnetizing inductance**

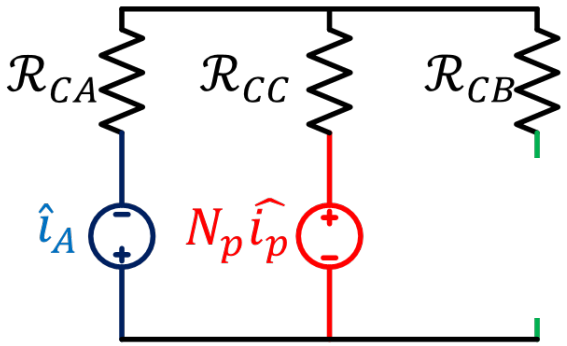
Comparison of Magnetic Circuit Models

- **In HB/0 Mode, half-bridge cells A2, B1, and B2 are bypassed while A1 remains switching**
- **In the limit where the switch on-resistance and ground plane resistance are negligible, the MMF of the rectifier B winding is modeled by a transference element which approaches an open circuit**

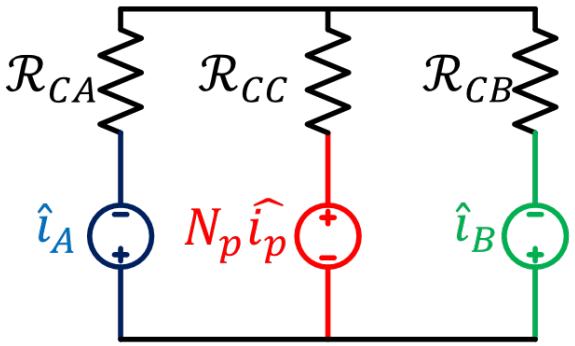
HB/0 Mode



Asymmetric Model

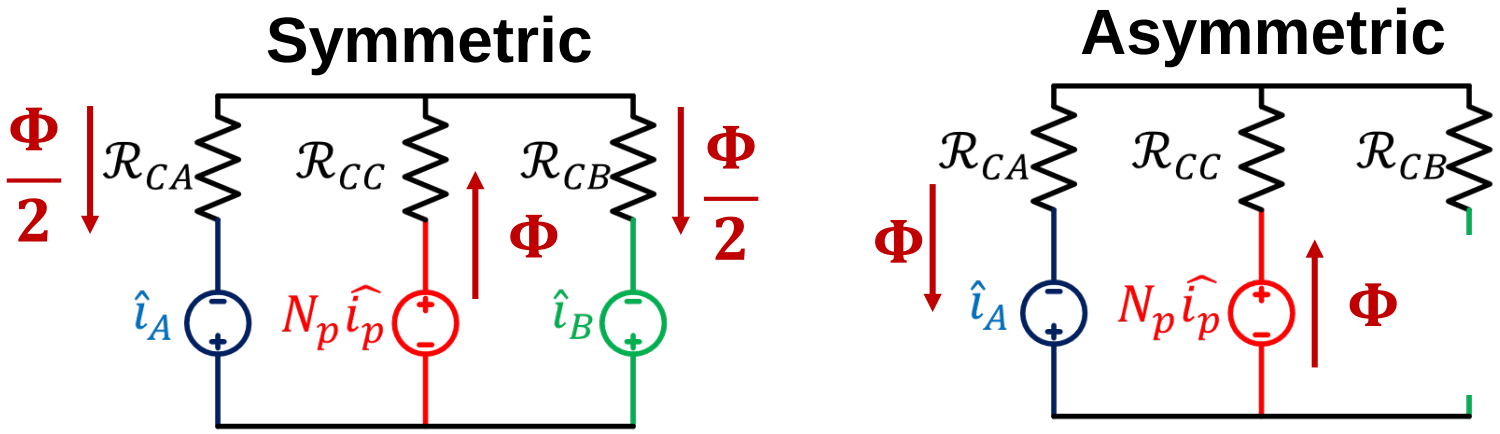


Symmetric Model



Increased Core Loss in HB/0 Mode

- **In HB/0 mode, the flux generated by the primary is ideally rejected from the right-side core leg**
- **Outer core leg must process all the flux, experiences up to twice the peak flux density compared to symmetric operation**
  - **This yields increased core loss due to superlinear dependence of core loss on flux density**



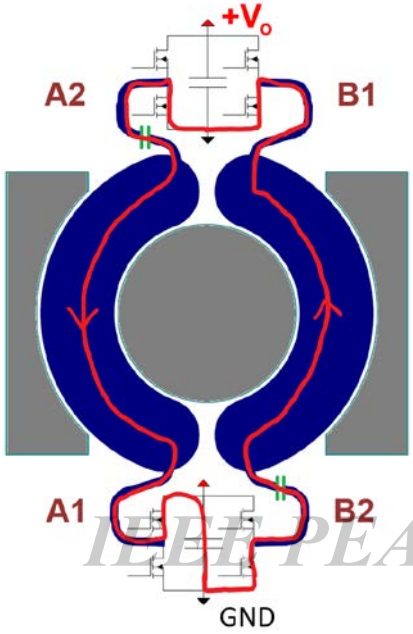
Symmetric vs. Asymmetric Operation

- **Symmetric Operation: Both rectifiers operated in an identical manner (i.e. FB/FB or HB/HB modes)**
- **Asymmetric Operation: Any other configuration (e.g. FB/HB, FB/0 or HB/0 modes)**
- **Compared to symmetric operation, asymmetric modes have worse core utilization**
- **Asymmetric-mode operation can be improved by**
  - **Optimization of core geometry for asymmetric mdoes**
  - **More advanced rectifier structures (e.g., “VIRT with Bypass”)**

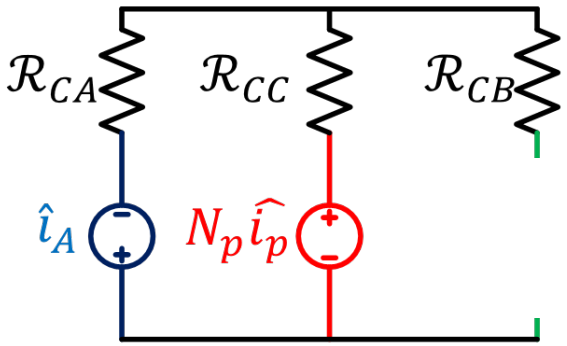
Comparison of Magnetic Circuit Models

- **In HB/0 Mode, half-bridge cells A2, B1, and B2 are bypassed while A1 remains switching**
- **In the limit where the switch on-resistance and ground plane resistance are negligible, the MMF of the rectifier B winding is modeled by a transference element which approaches an open circuit**

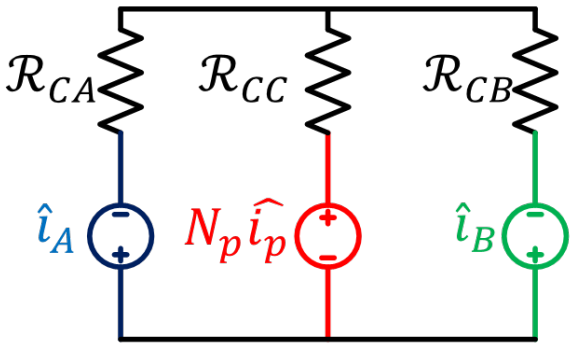
HB/0 Mode



Asymmetric Model



Symmetric Model



Increased Core Loss in HB/0 Mode

- **In HB/0 mode, the flux generated by the primary is ideally rejected from the right-side core leg**
- **Outer core leg must process all the flux, experiences up to twice the peak flux density compared to symmetric operation**
  - **This yields increased core loss due to superlinear dependence of core loss on flux density**